

Compal Confidential

V15 /DH5VF

V17 /DH7VF

Vx15/DH53F

Vx17/DH73F

MB Schematic Document

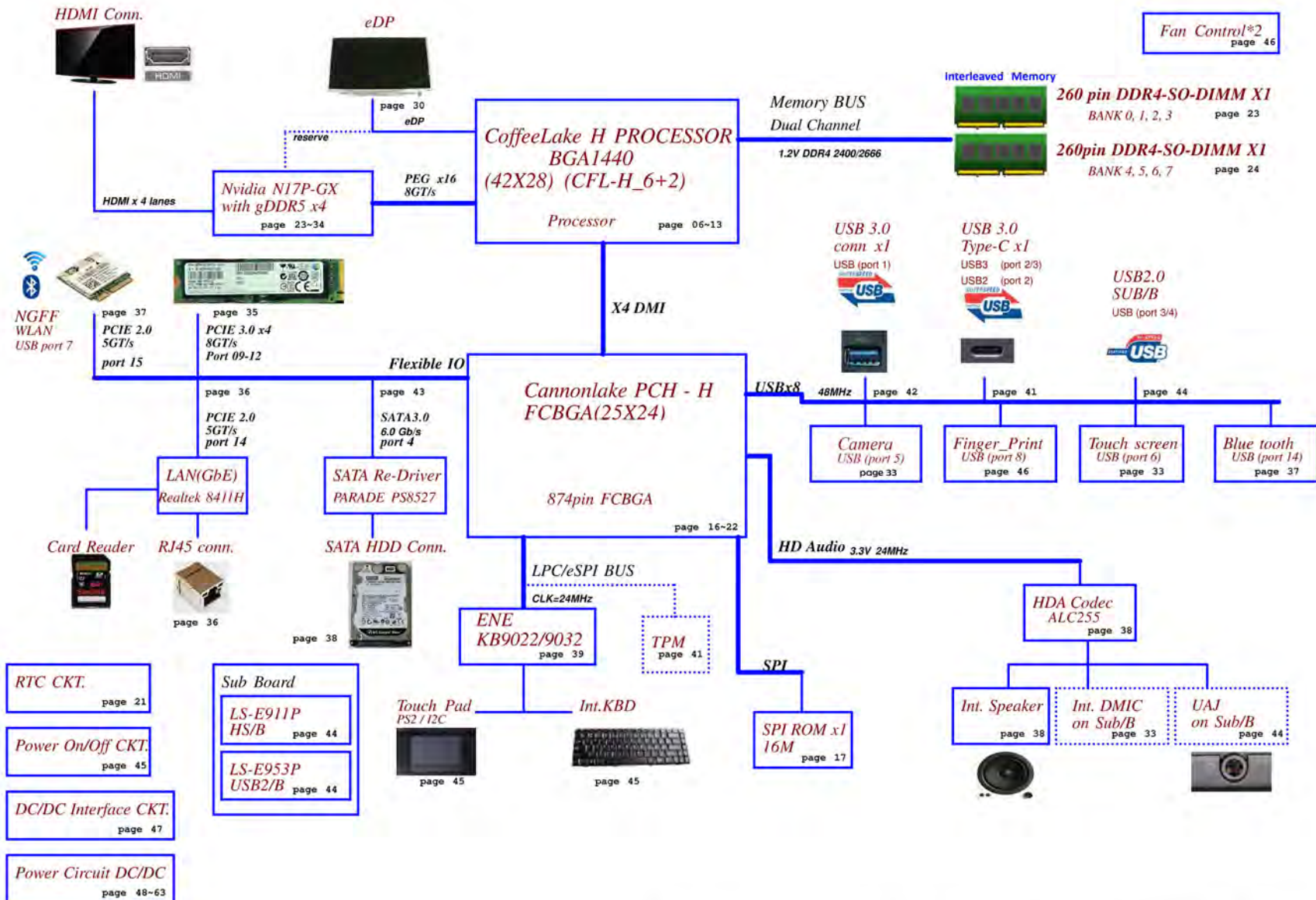
Intel CoffeeLake H
Nvidia N17P-G0/G1

LA-F951P

Rev:1A

2018.02.22

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Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	Cover Sheet
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Custom	DH5VF M/B LA-F591PR01	1.0		
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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{DD} min	V _{DD} typ	V _{DD} max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xFF
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Touch Panel	reserved		
I2C_1 (+3VS)	TM-P2969-001 (Touch Pad)			
	SB8787-1200 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
	LIS3DHTR(G-sensor)	0x30		
PCH_SML1CLK (+3VS)	N17P-GX (VGA)	0x9E		
	EC			
	CC controller 179F			
	TMS			
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

43 level BOM table

43 Level	Description	BOM Structure
Vx15, Sienta		
43IAB1B0L60	SMT MB AF951 DH53F I5QP89 PG1 4G 32HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I7#/G1#/VX15#/SATANRD#/
43IAB1B0L61	SMT MB AF951 DH53F I7QP86 PG1 4G 32HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I7#/G1#/VX17#/SATANRD#/
43IAB1B0L66	SMT MB AF951 DH53F I78750 PG1 4G 32HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I7#/G1#/VX15#/SATANRD#/
V15, Vx15-Fresd		
43IAB1B0L62	SMT MB AF951 DH53F I3QP89 PG0 4G 28HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I5#/G0#/V15#/SATANRD#/FP#
43IAB1B0L63	SMT MB AF951 DH53F I78750 PG0 4G 28HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I7#/G0#/V15#/SATANRD#/FP#
43IAB1B0L64	SMT MB AF951 DH53F I5QP89 PG1 4G 28HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I5#/G1#/V15#/SATANRD#/FP#
43IAB1B0L65	SMT MB AF951 DH53F I78750 PG1 4G 28HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I7#/G1#/V15#/SATANRD#/FP#
V17		
43IAB1B0L65	SMT MB AF951 DH7VF I5QP89 PG0 4G 28HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I5#/G0#/V15#/SATANRD#/FP#
43IAB1B0L65	SMT MB AF951 DH7VF I78750 PG0 4G 28HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I7#/G0#/V15#/SATANRD#/FP#
43IAB1B0L65	SMT MB AF951 DH7VF I5QP89 PG1 4G 28HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I5#/G1#/V15#/SATANRD#/FP#
43IAB1B0L65	SMT MB AF951 DH7VF I78750 PG1 4G 28HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I7#/G1#/V15#/SATANRD#/FP#
VX17		
43IAB1B0L68	SMT MB AF951 DH7VF I5QP89 PG1 4G 32HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I7#/G1#/V15#/SATANRD#/FP#
43IAB1B0L69	SMT MB AF951 DH7VF I78750 PG1 4G 32HDM1	255#/CHG#/CMC#/CNV1#/LD0#/IOAC#/TYPEC#/VGA#/QNDQ#/I7#/G1#/V15#/SATANRD#/FP#

X76730BOL51 SAMSUNG1280
X76730BOL52 HYNIX1280
X76730BOL53 SAMSUNG2560
X76730BOL54 HYNIX2560
X76730BOL55 MICRON2560

BOM Structure Table

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
CMC	CMC@
dGPU circuit	VGA@
VRAM BOM Select	X76@
TPM	TPM@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
USB charger	CHG@
non USB charger	NCHG@
G-Sensor	GSEN@
Thermal sensor	TMS@
for SW debug board	UART@
Intel CNVi (reserve)	CNVi@
Finger Print	FP@
FingerPrint(with PBA)	PBA@
USB Type-C CC controller	TYPEC@
EMI/ESD requirement	EMC@
EMI/ESD require reserve	XEMC@
FP ESD requirement	FPEMC@
28P keyboard connector	V15@
32P keyboard connector	VX15@
SATA HDD W REDRIVER	SATARD@
SATA HDD WO REDRIVER	SATANRD@
NV N17P-G0(1050)	G0@
NV N17P-G1(1050TI)	G1@
i5 CPU	I5@
i7 CPU	I7@
ALC 255 Codec	255@
ALC 256 Codec	256@
Codec LDO mode	LDO@
Codec Switch mode	SWR@

State

SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
	HIGH	HIGH	HIGH	ON	ON	ON	ON
RAM	LOW	HIGH	HIGH	ON	ON	OFF	OFF
Disk	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

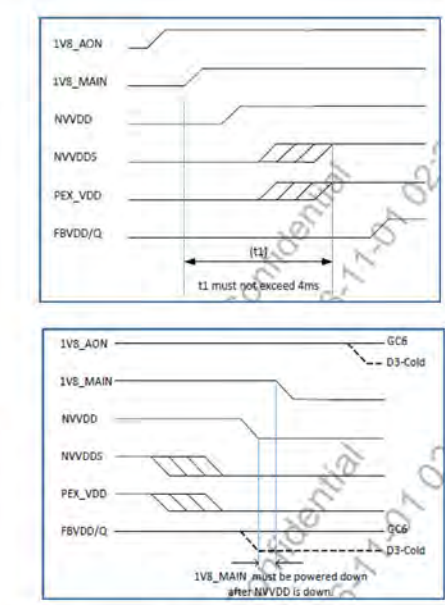
Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH_PRIM	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator.	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.9VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+1.8VGA_CORE	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

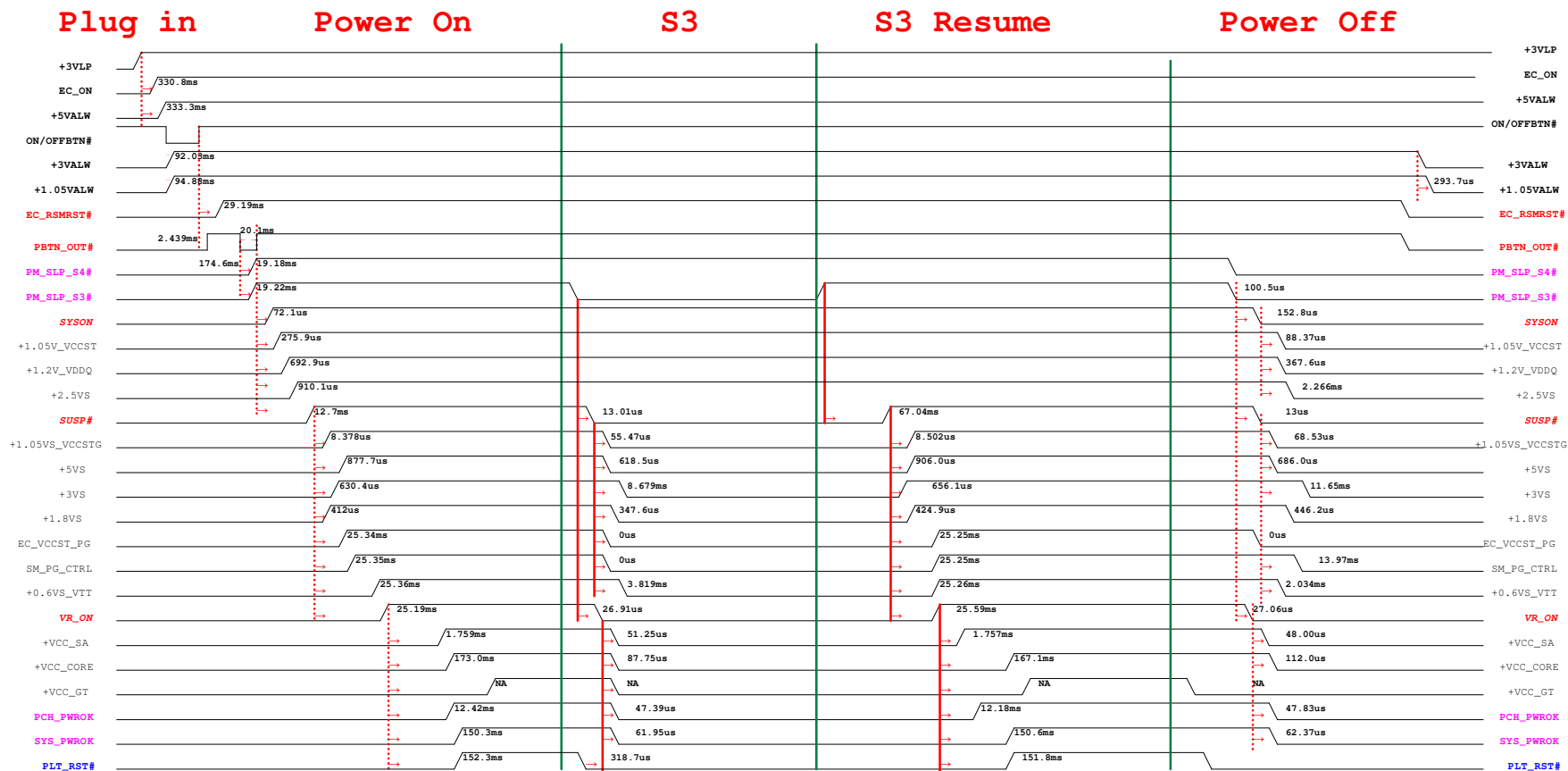
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

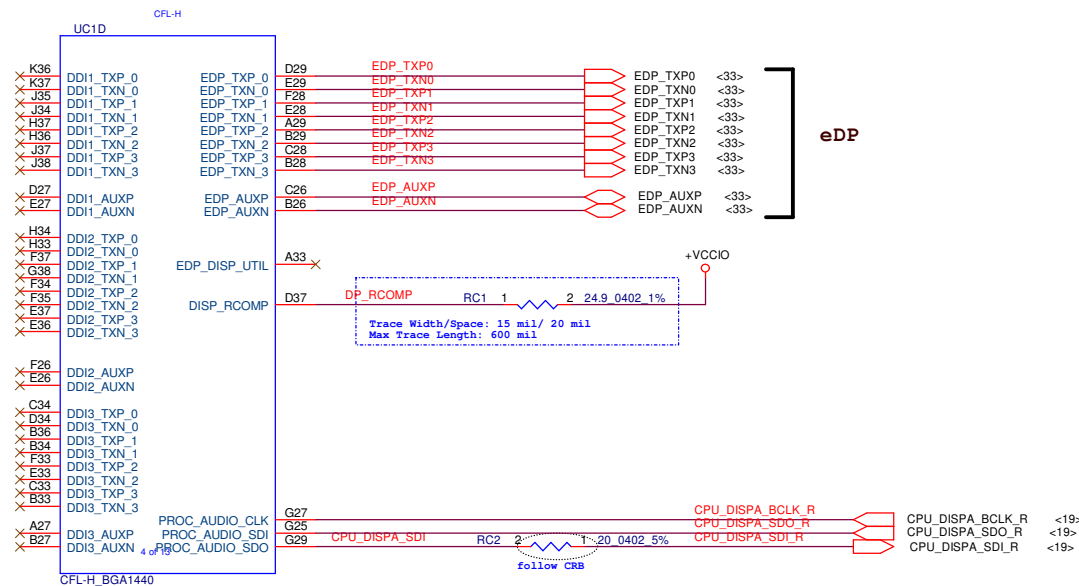
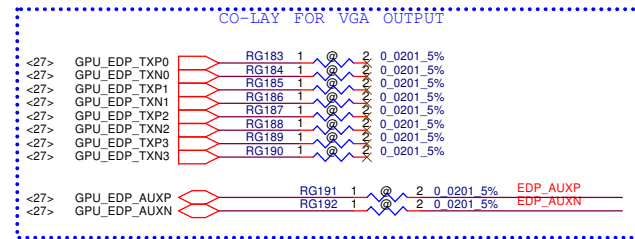
BOARD ID Table

V series		Vx series	
Board ID	PCB Revision	Board ID	PCB Revision
0	0.1	10	0.1
1	0.2	11	0.2
2	1.0	12	1.0
3	1.A	13	1.A
4		14	
5	1.0	15	1.0
6		16	
7		17	
8		18	
9		19	

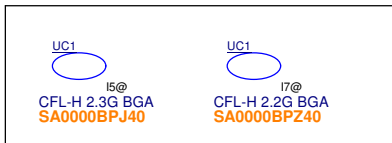
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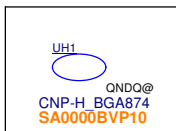
BIOS ver: V0.02W1
EC: ver: V002AT04



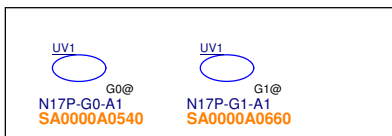
Coffee Lake-H CPU SKU



Cannon Lake PCH SKU



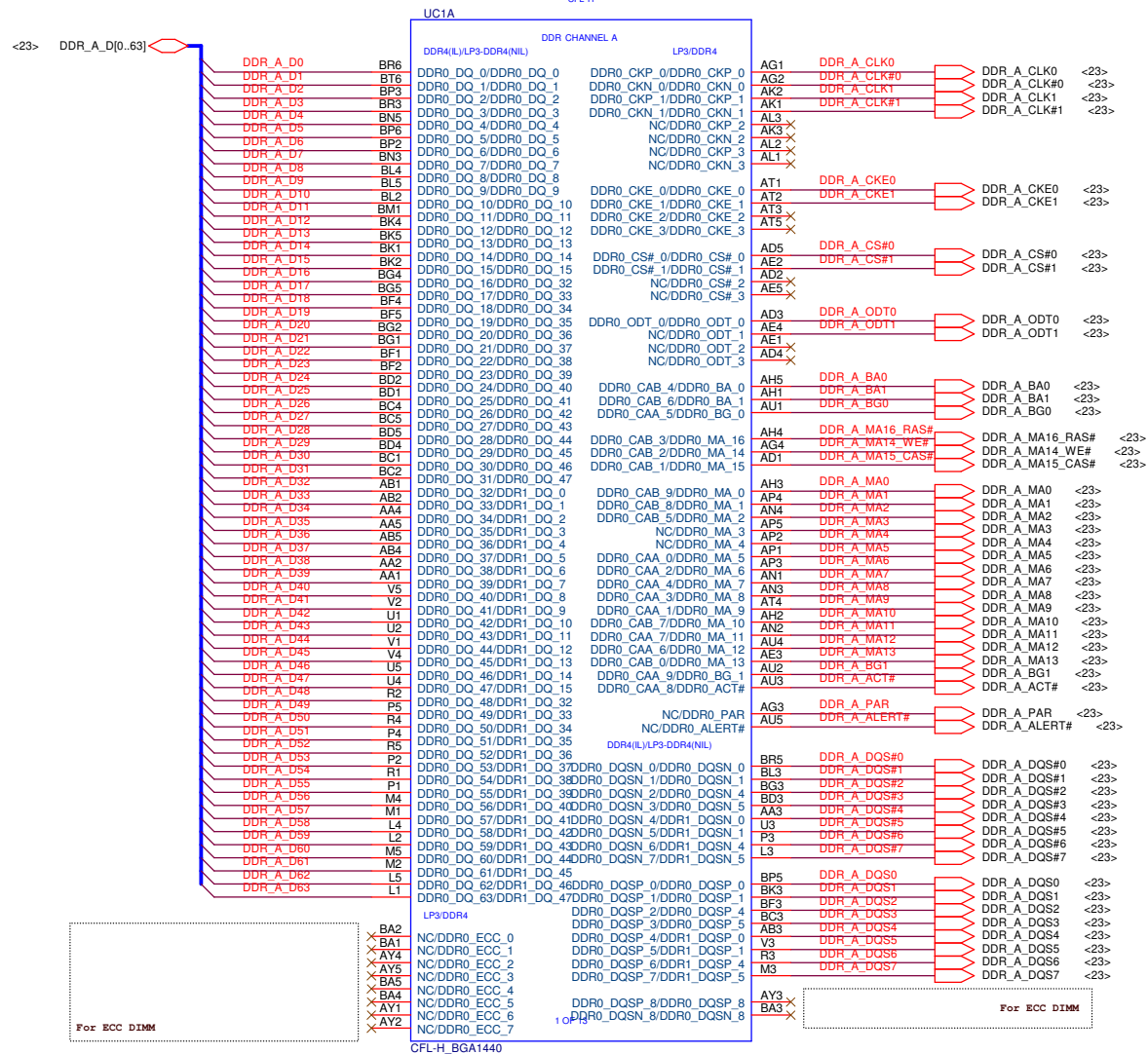
NV N17P SKU



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				CFL-H(1/8)DDI/eDP	
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CHANNEL-A

Interleaved Memory



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PEG&DMI

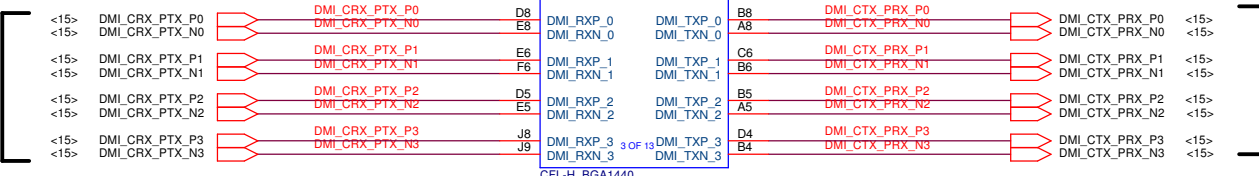
To DGPU
PEG Lane Reversed

To DGPU
PEG Lane Reversed



To PCH

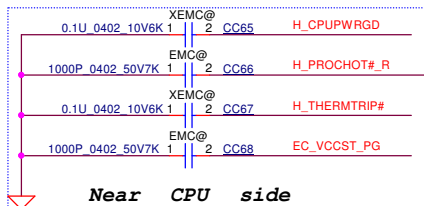
To PCH



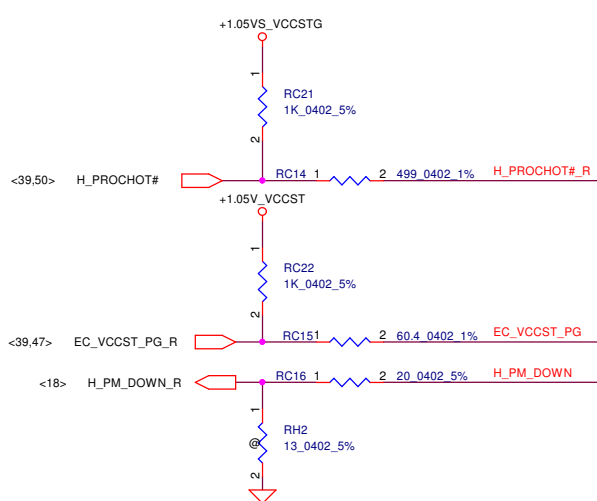
571391_CFL_H_PDG_Rev0p5
 1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
 2. Route the Alert signal between the Clock and the Data signals.
 3. Place those resistors close CPU side.



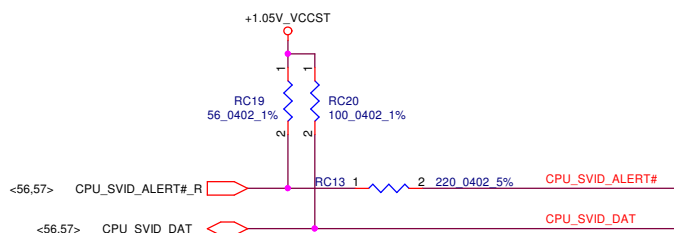
PROC_SELECT#
 should be unconnected on CFL processor
 EDS1.2 8/21



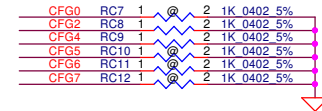
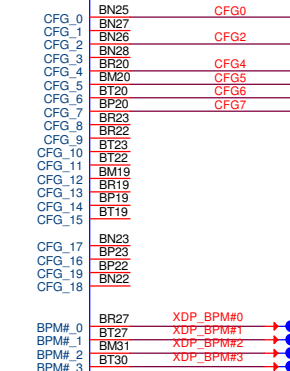
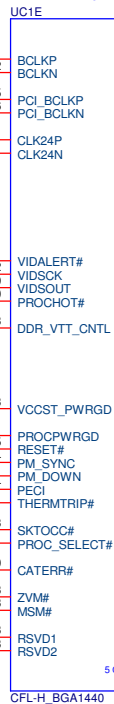
Near CPU side
 follow 1050 Request
 8/21



SVID

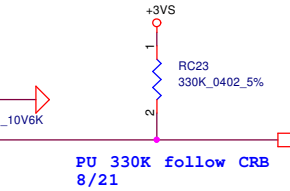
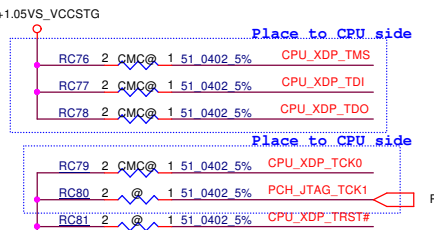
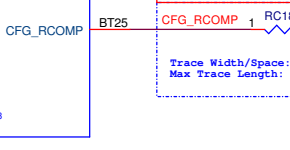
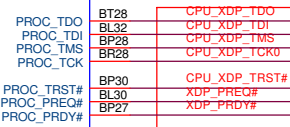


CFL-H



The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted
* 1 = (Default) Normal Operation;
0 = Stall.
CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed.
CFG[4]: eDP enable:
1 = Disabled.
0 = Enabled.
CFG[6:5]: PCI Express* Bifurcation:
00 = 1 x8, 2 x4 PCI Express*
01 = reserved
10 = 2 x8 PCI Express*
11 = 1 x16 PCI Express*
CFG[7]: PEG Training:
* 1 = (default) PEG Train immediately following RESET# de assertion.
0 = PEG Wait for BIOS for training.
*CFG Pin Use CMC debug on DDX03 R02 Schematic.



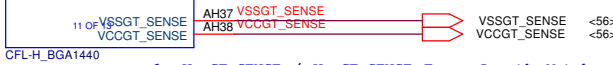
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Compal Electronics, Inc.	
CFL-H(5/8)CFG,SVID	

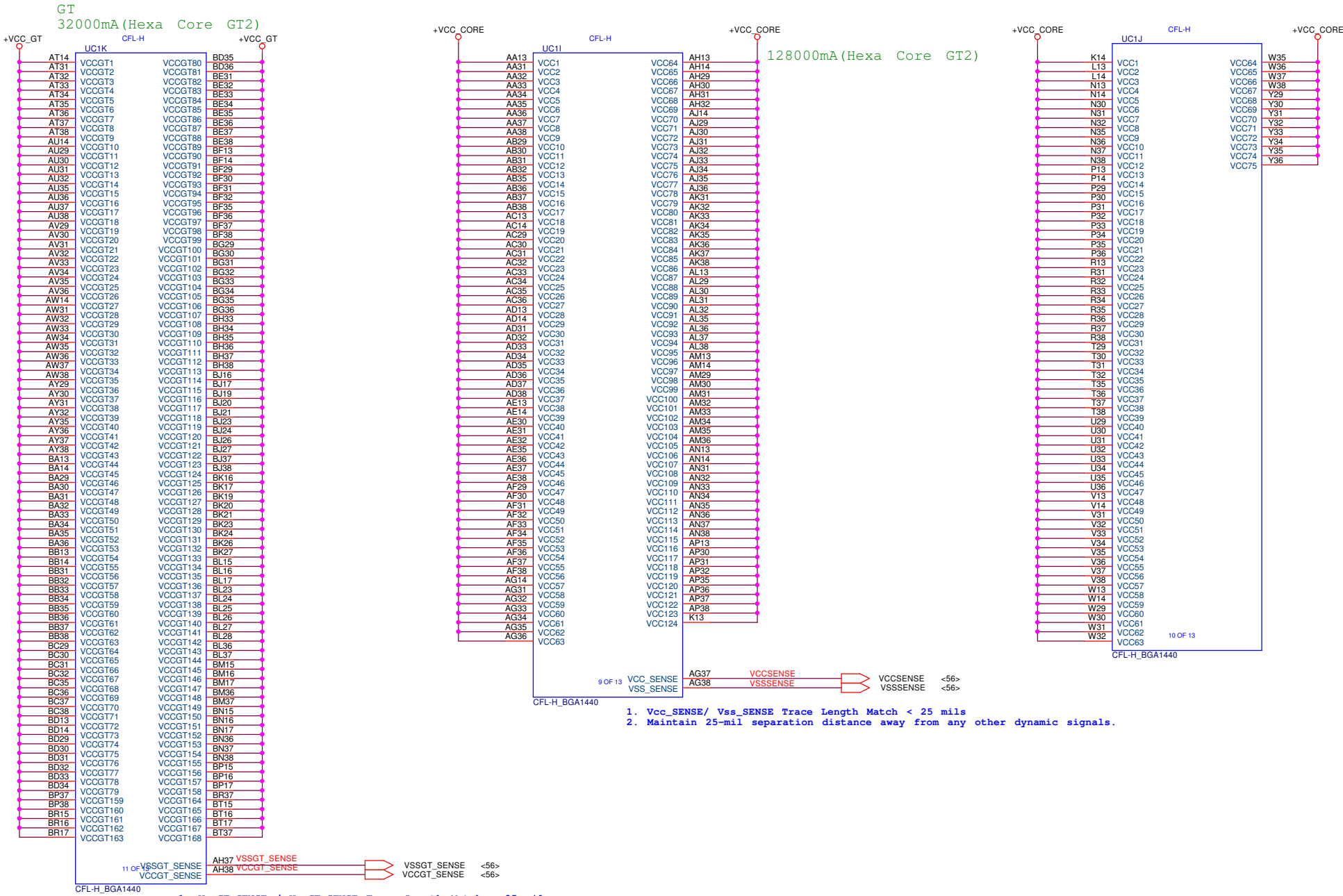
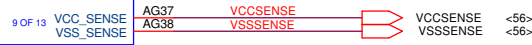
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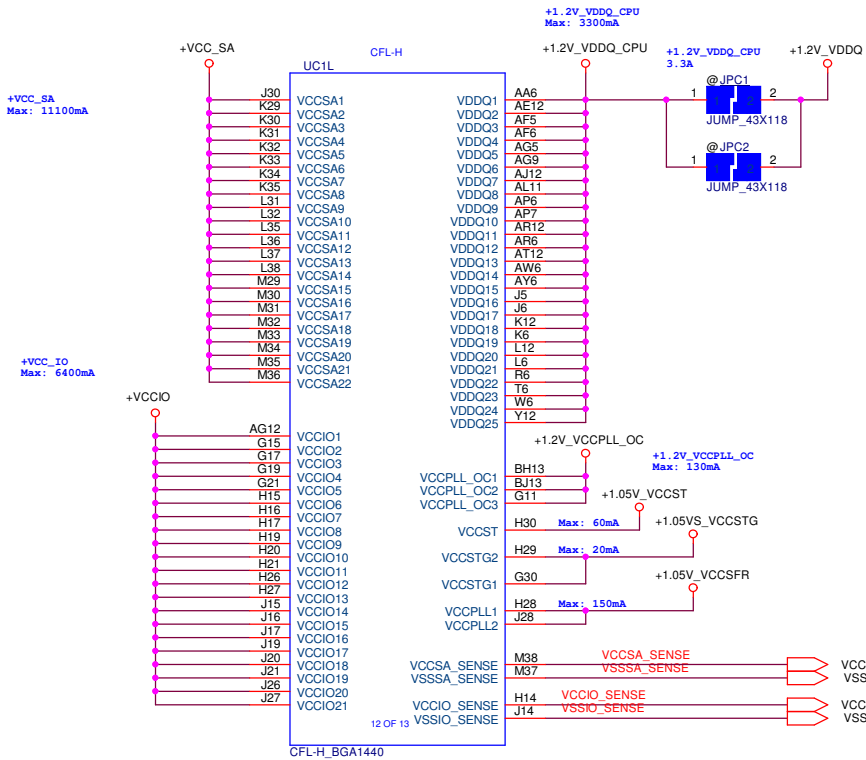
WWW.ALISALER.COM

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

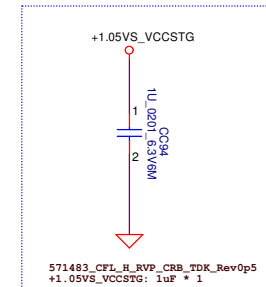
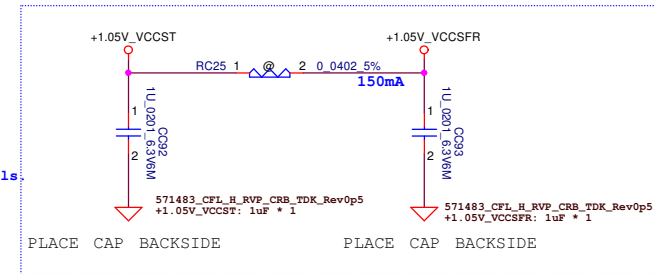
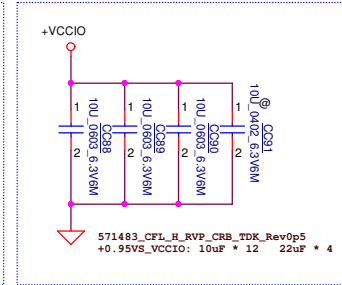
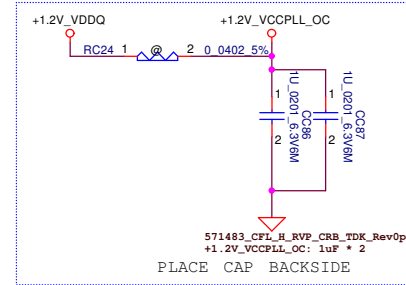
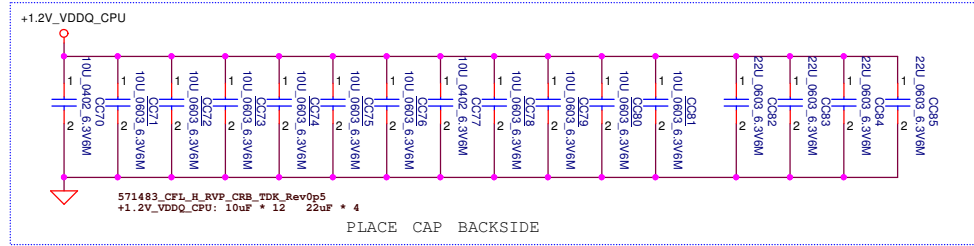


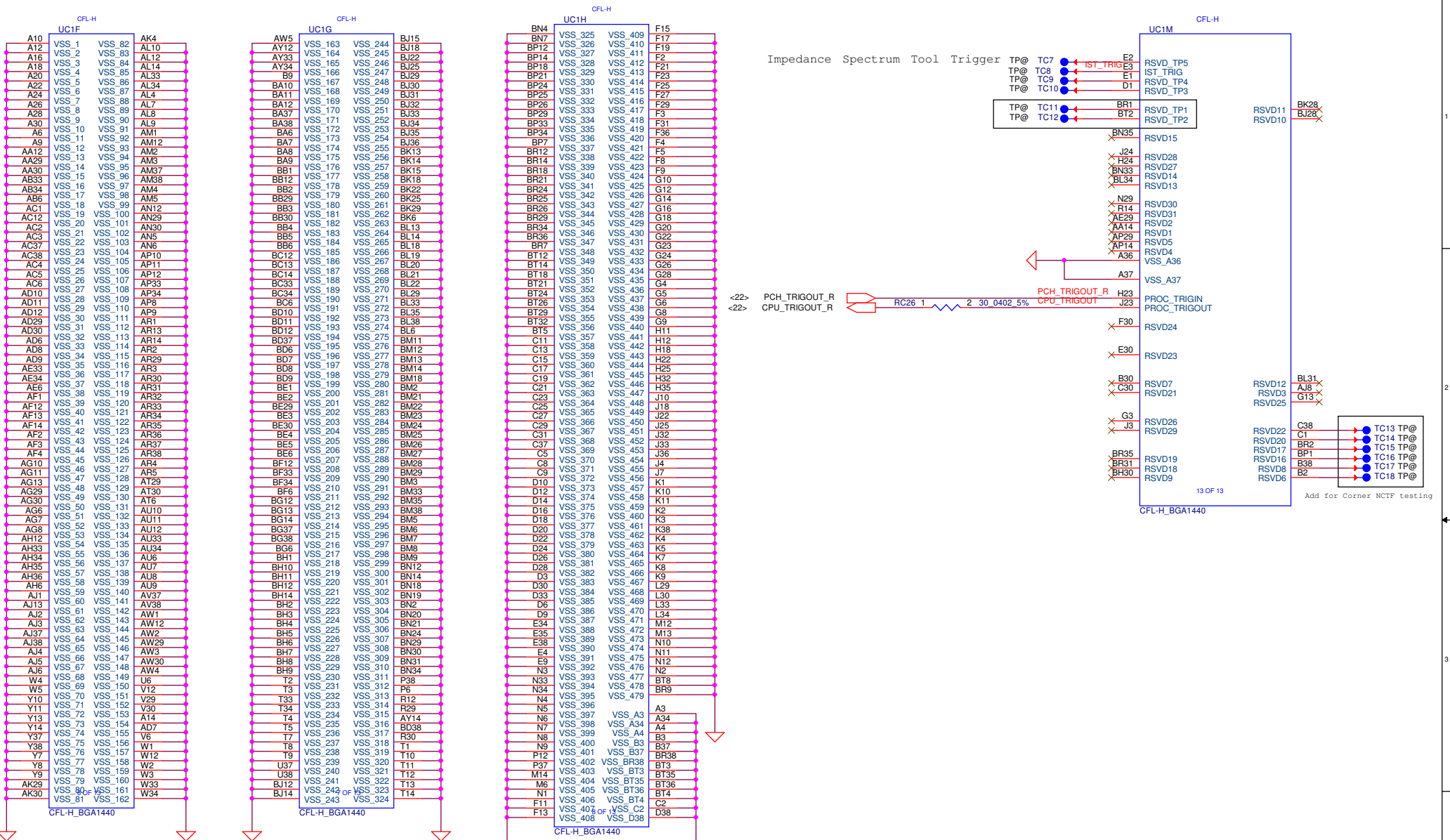
1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

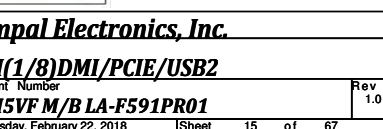
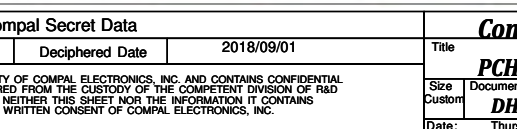
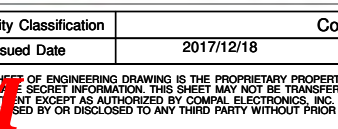
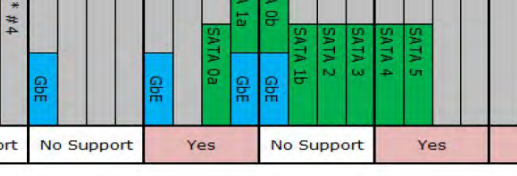
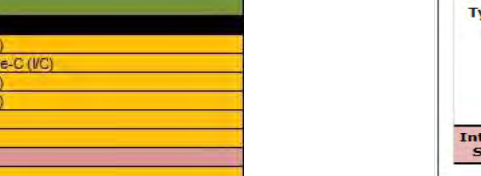
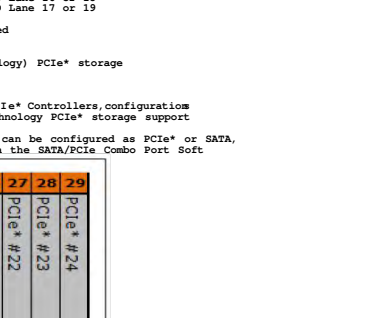
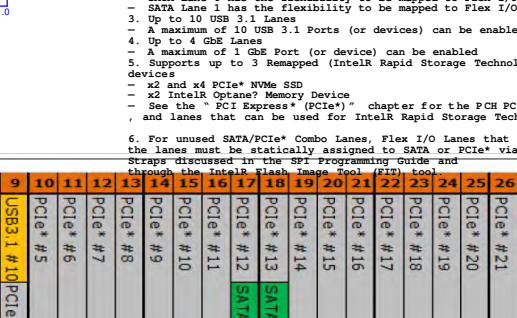
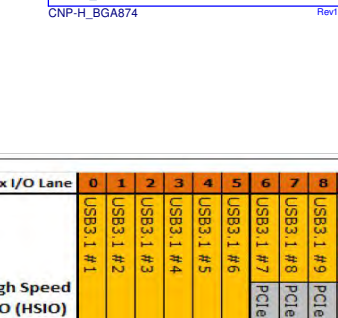
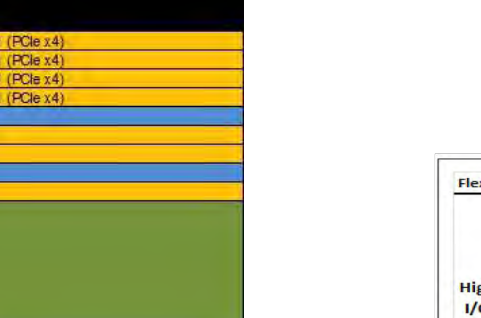
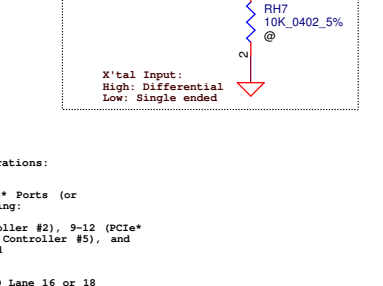
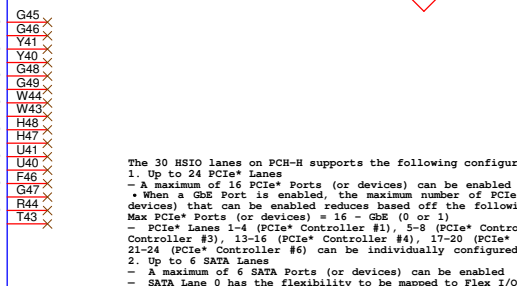
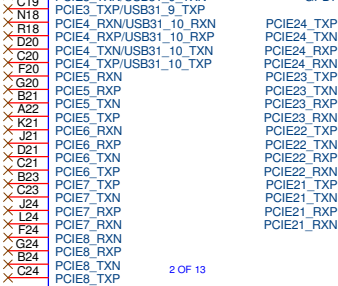
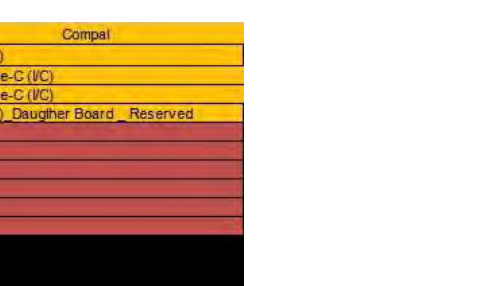
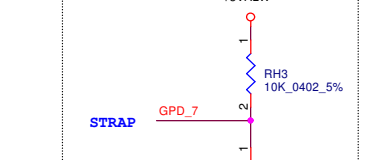
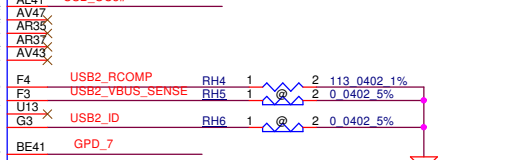
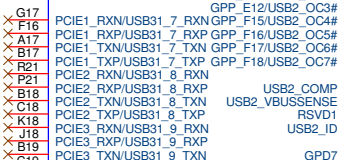
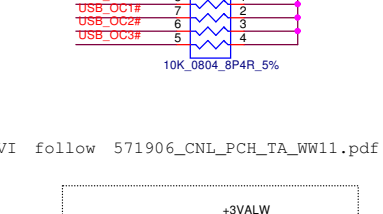
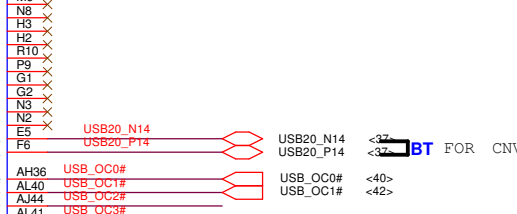
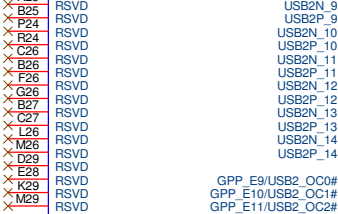
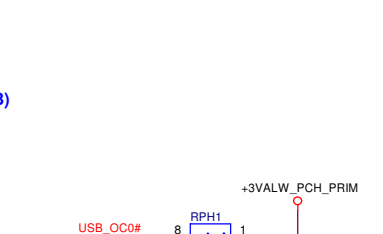
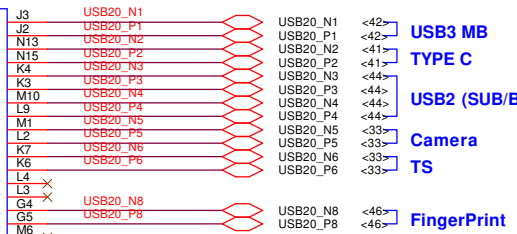
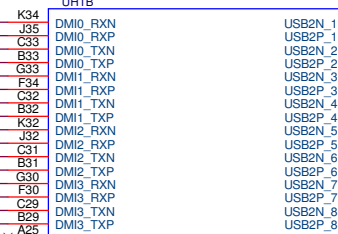
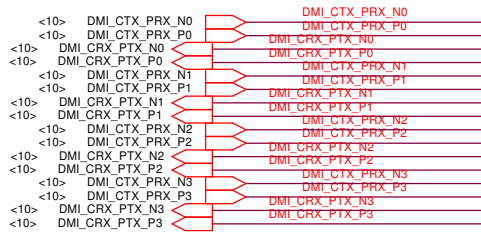




1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.







CPL-H (HM370)		Compal	
Lane0	USB3.1 Port1		USB 3 (I/O)
Lane1	USB3.1 Port2		USB 3 Type-C (I/C)
Lane2	USB3.1 Port3		USB 3 Type-C (I/C)
Lane3	USB3.1 Port4		USB 3 (I/O) Daughter Board Reserved
Lane4	USB3.1 Port5		
Lane5	USB3.1 Port6		
Lane6	USB3.1 Port7	PCle Port1	
Lane7	USB3.1 Port8	PCle Port2	
Lane8	USB3.1 Port9	PCle Port3	
Lane9	USB3.1 Port10	PCle Port4	
Lane10		PCle Port5	
Lane11		PCle Port6	
Lane12		PCle Port7	
Lane13		PCle Port8	
Lane14		PCle Port9	M.2 SSD#1 (PCle x4)
Lane15		PCle Port10	M.2 SSD#1 (PCle x4)
Lane16	SATA3 Port0	PCle Port11	M.2 SSD#1 (PCle x4)
Lane17	SATA3 Port1	PCle Port12	M.2 SSD#1 (PCle x4)
Lane18	SATA3 Port0*	PCle Port13	
Lane19	SATA3 Port1*	PCle Port14	LAN+CR
Lane20	SATA3 Port2	PCle Port15	WIFI
Lane21	SATA3 Port3	PCle Port16	
Lane22	SATA3 Port4	PCle Port17	HDD
Lane23	SATA3 Port5	PCle Port18	
Lane24		PCle Port19	
Lane25		PCle Port20	
Lane26		PCle Port21	
Lane27		PCle Port22	
Lane28		PCle Port23	
Lane29		PCle Port24	
USB2 Port1			USB 3 (I/O)
USB2 Port2			USB 3 Type-C (I/C)
USB2 Port3			USB 2 (I/O)
USB2 Port4			USB 2 (I/O)
USB2 Port5			CCD
USB2 Port6			TS
USB2 Port7			
USB2 Port8			FP
USB2 Port9			
USB2 Port10			
USB2 Port11			
USB2 Port12			
USB2 Port13			
USB2 Port14			
USB2 Port15			
USB2 Port16			
USB2 Port17			
USB2 Port18			
USB2 Port19			
USB2 Port20			
USB2 Port21			
USB2 Port22			
USB2 Port23			
USB2 Port24			

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCle #5	PCle #6	PCle #7	PCle #8	PCle #9	PCle #10	PCle #11	PCle #12	SATA 1a	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5	SATA 6	SATA 7	SATA 8	SATA 9	SATA 10	SATA 11
High Speed I/O (HSIO) Type and Lane																														
Intel® RST Support											No Support	No Support																		

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2017/12/18		Deciphered Date	
				2018/09/01	
Title		PCH(1/8)DMI/PCIE/USB2		Rev 1.0	
Size		Document Number		Date	
Custom		DH5VF M/B LA-F591PR01		Thursday, February 22, 2018	
Date		Sheet		15 of 67	

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can remove if no use DP
08/18

remove PCH DP SCLK/SDATA

DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B-D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after
PCH_PWRON de-asserts.
2. This signal is in the primary well.

no follow naming
<25,34> HDMI_HPD_PCH
<25,33> EDP_HPD

<36,39>

EC_PME#

EC_PME#_R

RH24

1

2

0.0402_5%

BE36

UH1A

GPP_A11/PME#/SD_VDD2_PWR_EN#

GPP_B13/PLTRST#

AV29

PLT_RST#

PLT_RST#

<25,39,45>

XEMC@

CH9

1

2

100P_0402_50V8J

PLT_RST#

RA1381

2

100K_0201_5%

intel critical net recommend

TP_INT#

RH28

2

1

100K_0402_5%

+3VS

TP_INT#

<39,45>

<40>

TYPEC_1P5A

EC_TP_INT#

TP_INT#

RH28

2

1

100K_0402_5%

+3VS

TP_INT#

<39,45>

<40>

TYPEC_1P5A

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TP_INT#

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<40>

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100K_0402_5%

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<40>

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100K_0402_5%

+3VS

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<40>

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TP_INT#

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<40>

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100K_0402_5%

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TP_INT#

RH28

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100K_0402_5%

+3VS

TP_INT#

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TYPEC_1P5A

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TP_INT#

RH28

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1

100K_0402_5%

+3VS

TP_INT#

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TYPEC_1P5A

EC_TP_INT#

TP_INT#

RH28

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1

100K_0402_5%

+3VS

TP_INT#

<39,45>

<40>

TYPEC_1P5A

EC_TP_INT#

TP_INT#

RH28

2

1

100K_0402_5%

+3VS

TP_INT#

<39,45>

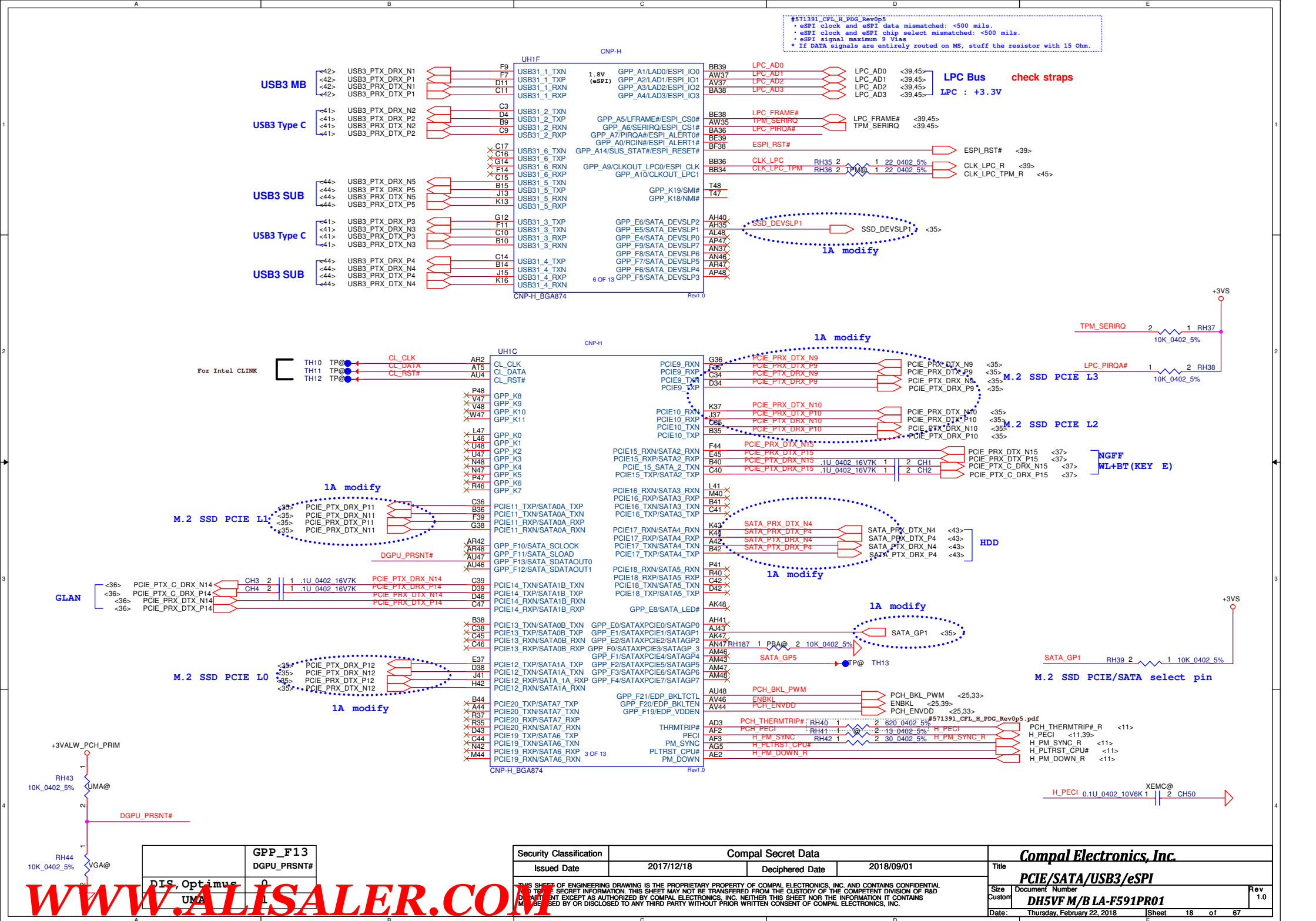
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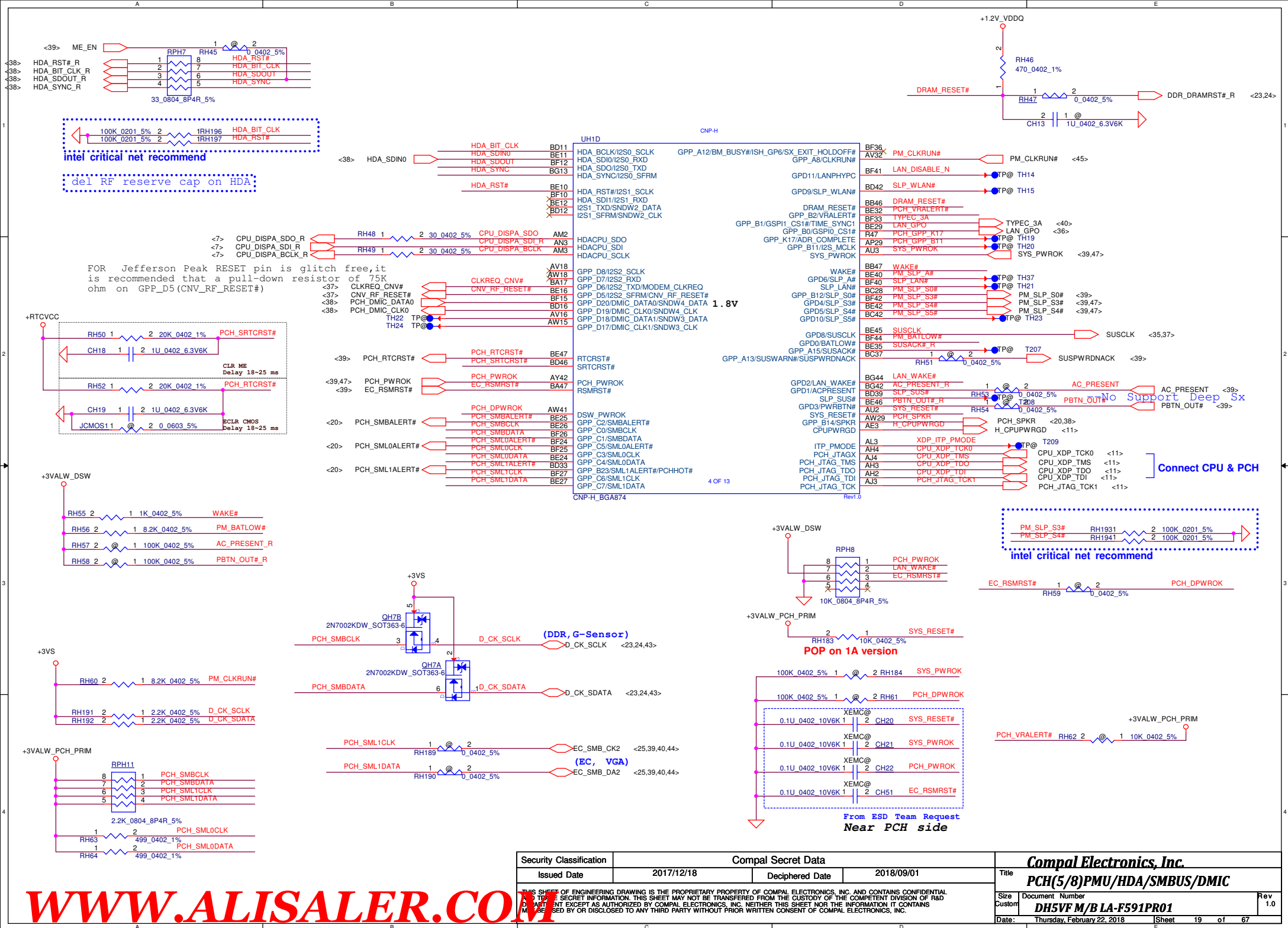
TYPEC_1P5A

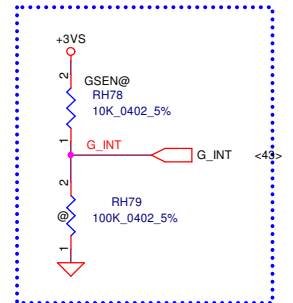
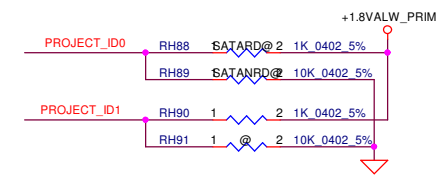
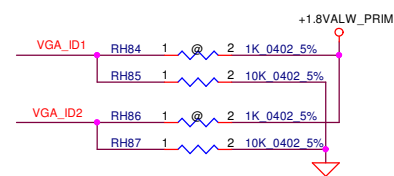
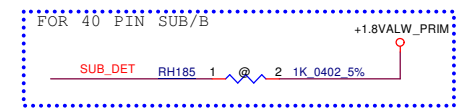
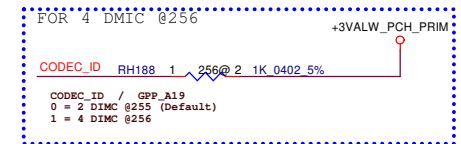
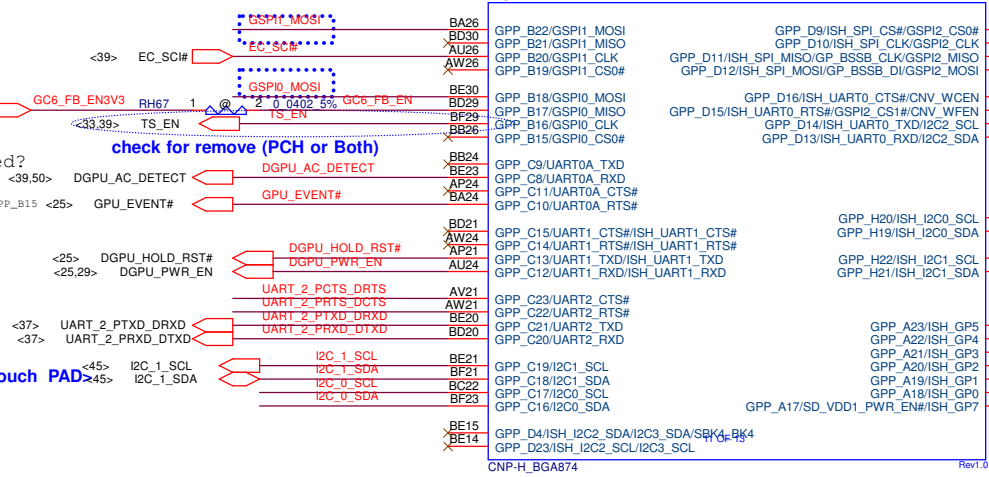
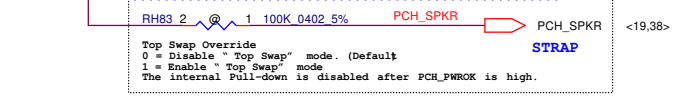
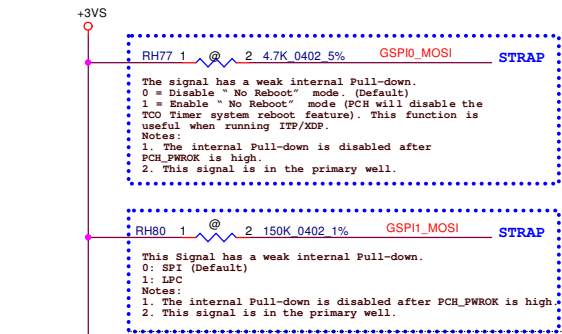
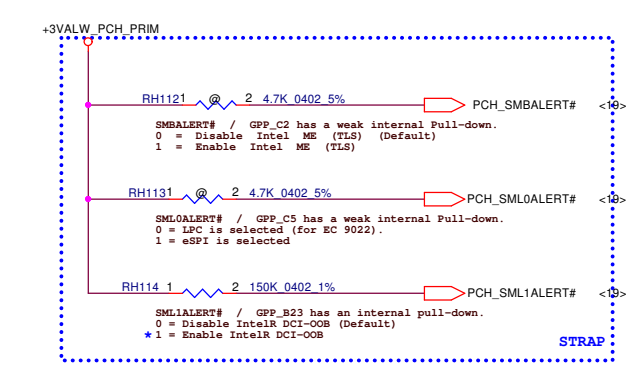
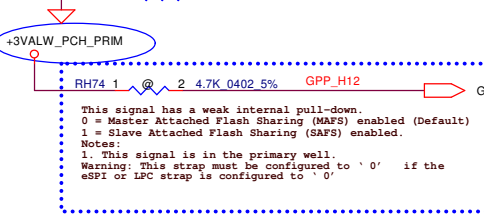
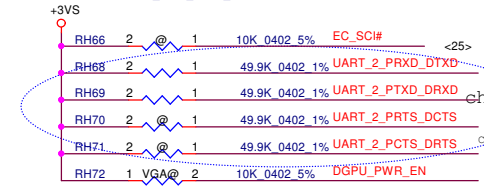
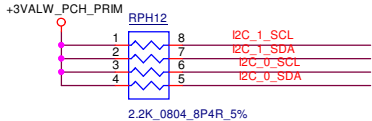
EC_TP_INT#

TP_INT#

RH







pop for avoid floating
1.0 Modify

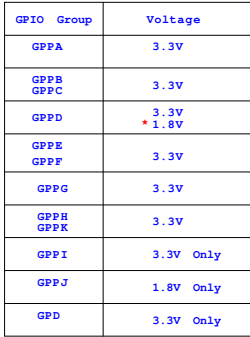
	GPP_D10	GPP_D9	Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
Reserved	0	0	DH53F(1060 WO RD)	0	0
Reserved	0	1	DH53F(1060 W RD)	0	1
Reserved	1	0	*DH5VF(1050 WO RD)	1	0
for 8 Layer	1	1	*DH5VF(1050 W RD)	1	1

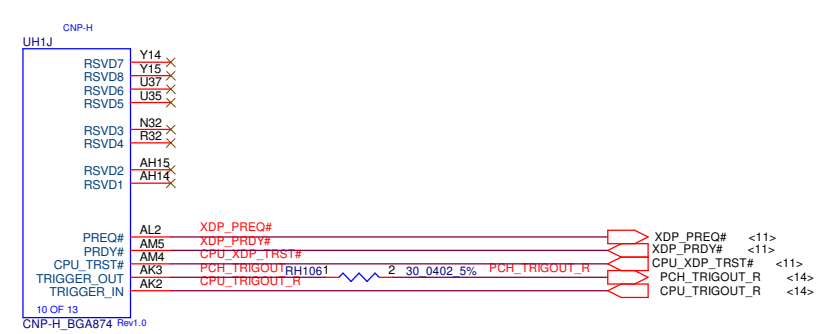
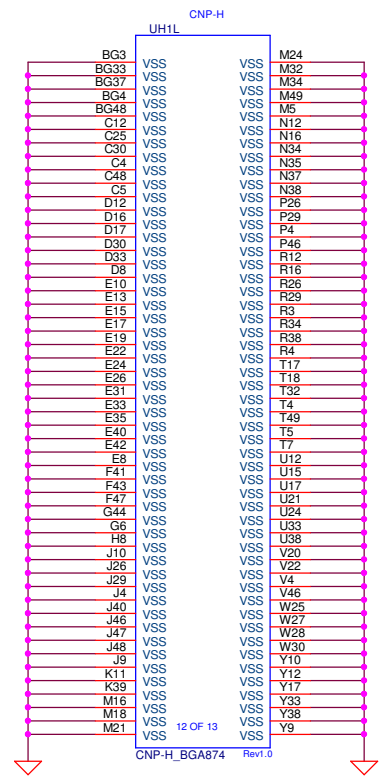
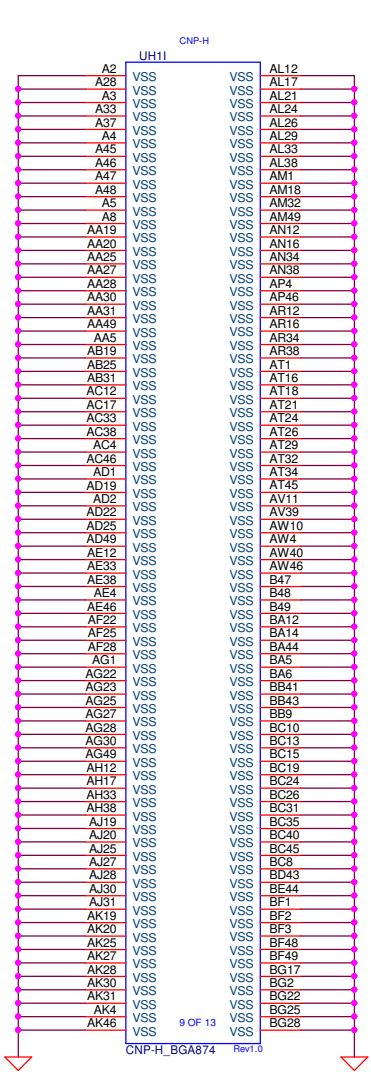
*note: 00/01 used or 1050
EVT
10 used for 1060 EVT

SCI capability is available on all GPIOs
PCH GPIOs that can be routed to generate SMI# or NMI:
• GPP_B14, GPP_B20, GPP_B23
• GPP_C[23:22]
• GPP_D[4:0]
• GPP_E[8:0]
• GPP_I[3:0]
• GPP_G[7:0] (support SMI# only).

The voltage of all GPIO pads in each GPP group is determined by the voltage supplied to the group (either 3.3V or 1.8V), except for GPP_I and GPP_D group, (which are 3.3V only), and GPP_J group (which is 1.8V only).

All GPIOs have programmable internal pull-up/pull-down resistors which are off by default.
The internal pull-up/pull-down for each GPIO can be enabled by BIOS programming.





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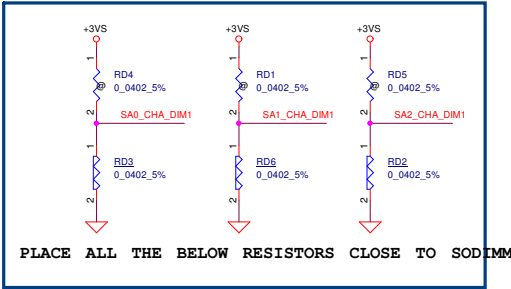
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Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	PCH(8/8)GND/RSVD
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D OR ANY OTHER DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS SHALL BE REPRODUCED, COPIED, OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number DH5VF M/B LA-F591PR01
				Date: Thursday, February 22, 2018	Sheet 22 of 67

CHANNEL-A

BOT REVERSE TYPE (4 mm)

Interleaved Memory

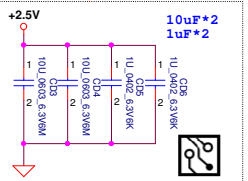
TOP: JDIMM1 CONN Non-ECC DIMM



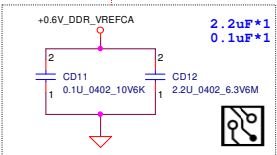
SPD ADDRESS FOR CHANNEL A :
 WRITE ADDRESS: 0XA0
 READ ADDRESS: 0XA1
 SA0 = 0; SA1 = 0; SA2 = 0.
 DDR4 POR OPERATING SPEED: 1867 MT/S
 STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

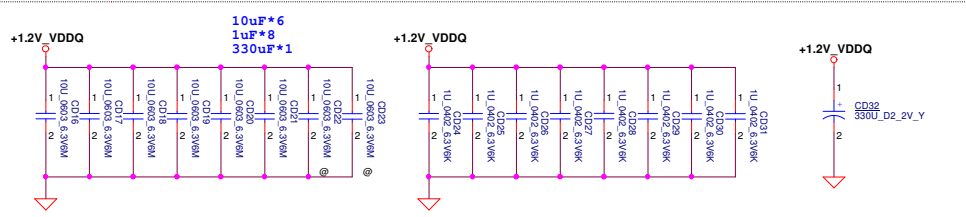
Layout Note:
Place near JDIMM1.258



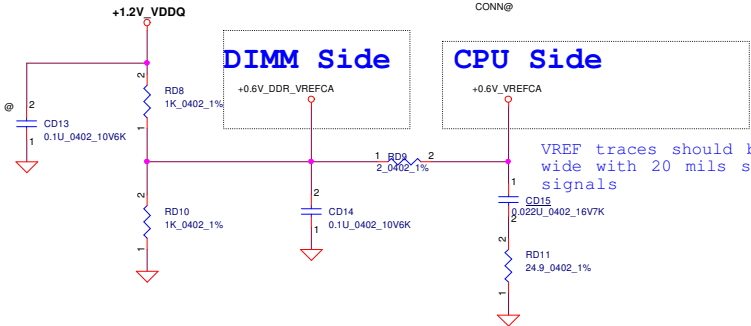
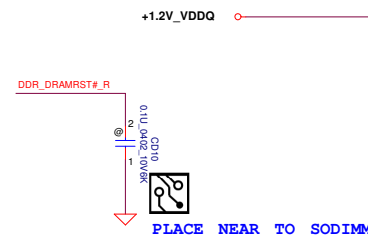
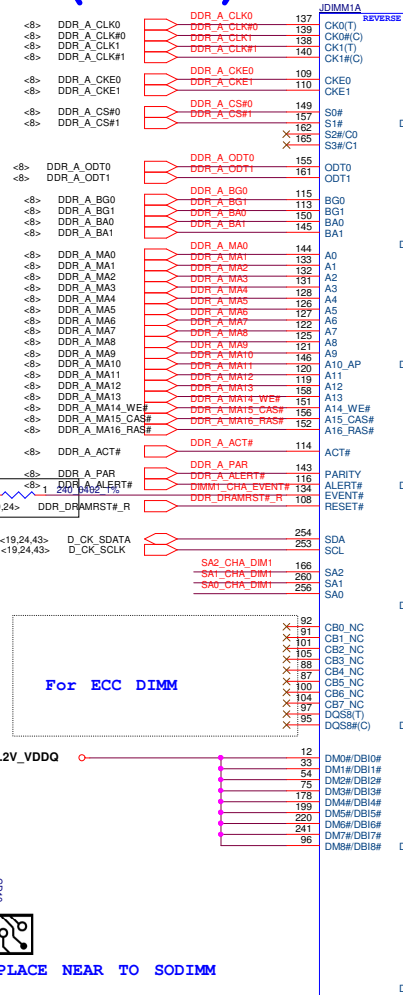
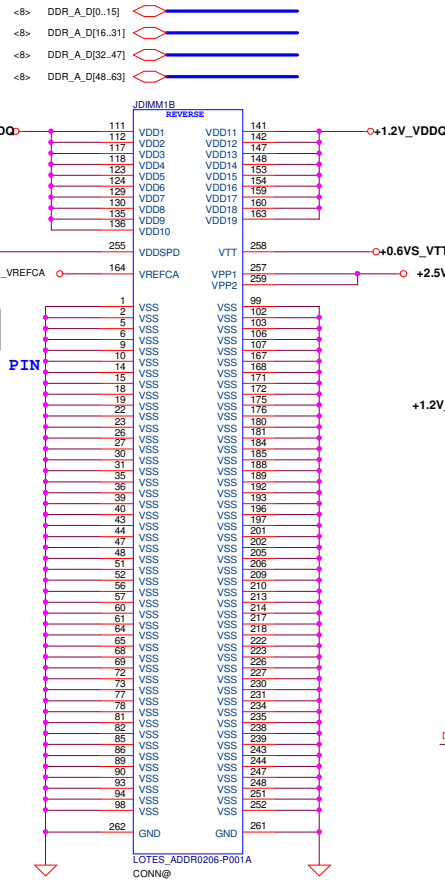
Layout Note:
PLACE THE CAP near JDIMM1.164



Layout Note:
Place near JDIMM1



Part Number:SP07001FYH0
 Part Value:S SOCKET FOX_AS0A826-H4RB-7H 260P DDR4



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

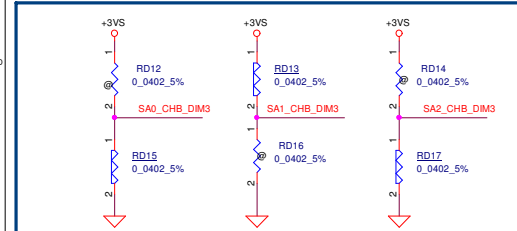
CHANNEL-B

BOT

STD (4 mm)

Interleaved Memory

TOP: JDIMM3 CONN Non-ECC DIMM

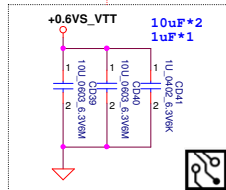
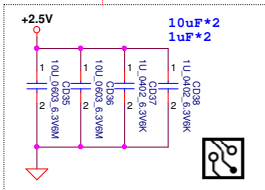


PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

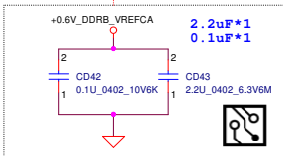
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM3.257,259

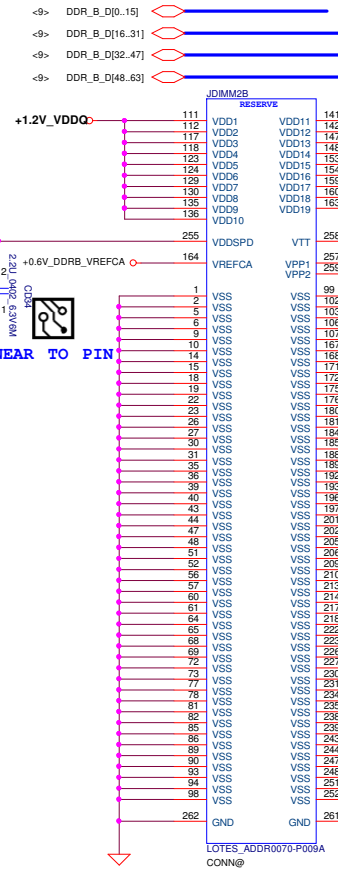
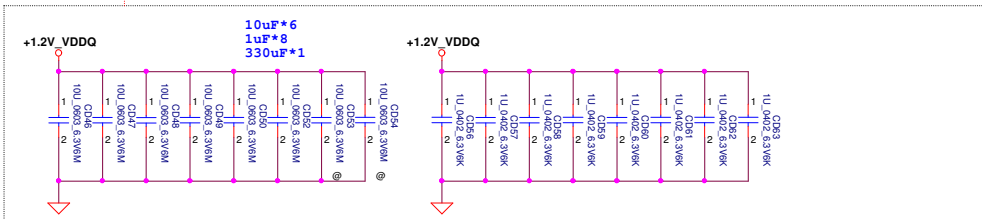
Layout Note:
Place near JDIMM3.258



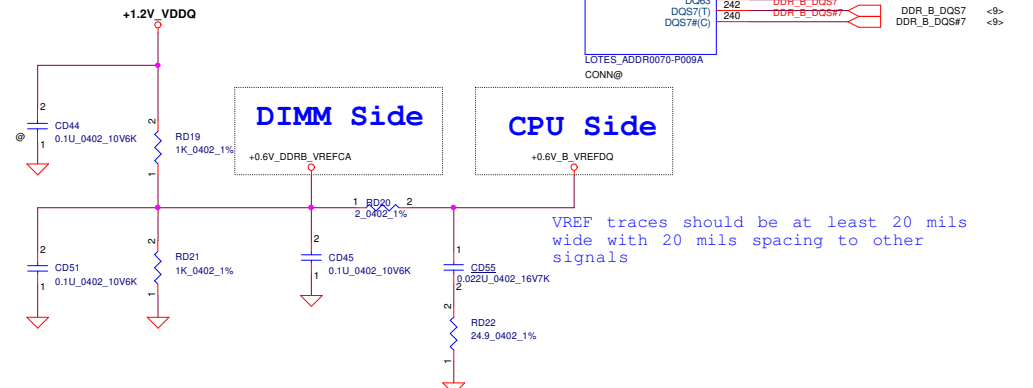
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM3



Layout Note:
Place near JDIMM3



Part Number:SP07001CEAO
Part Value:S SOCKET FOX_AS0A826-H4SB-7H 260P DDR4



For ECC DIMM

+1.2V_VDDQ

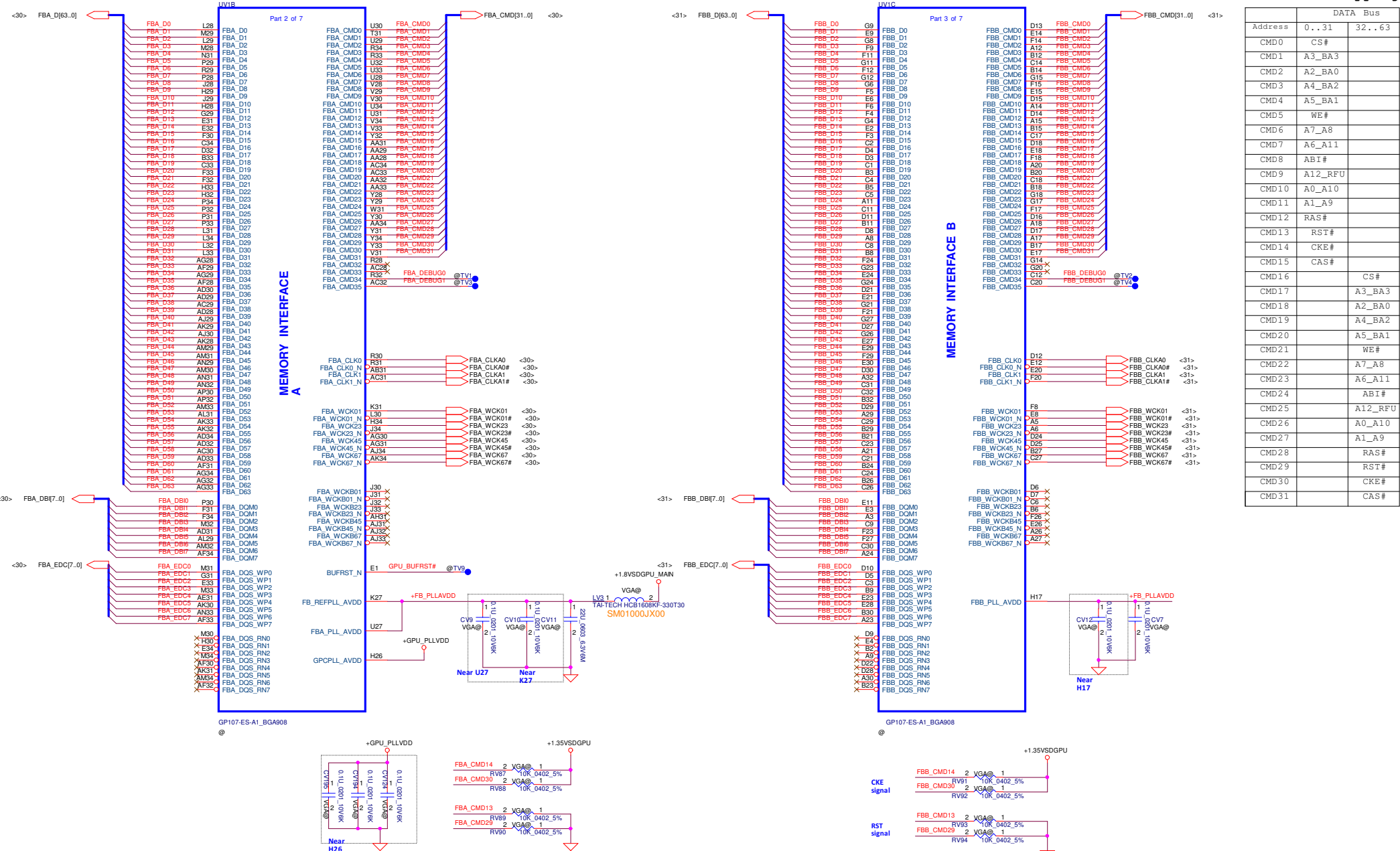
+1.2V_VDDQ

DIMM Side

CPU Side

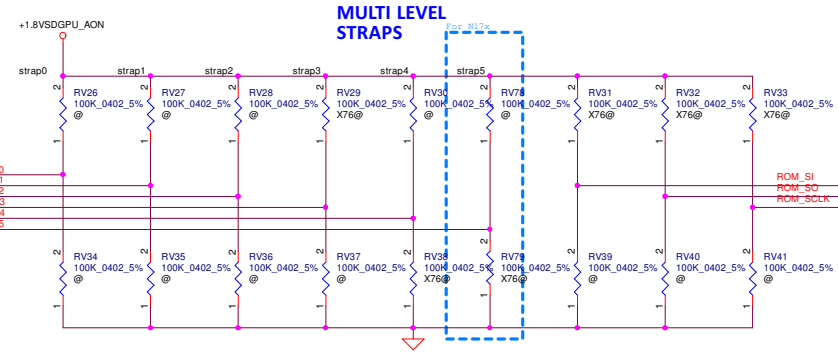
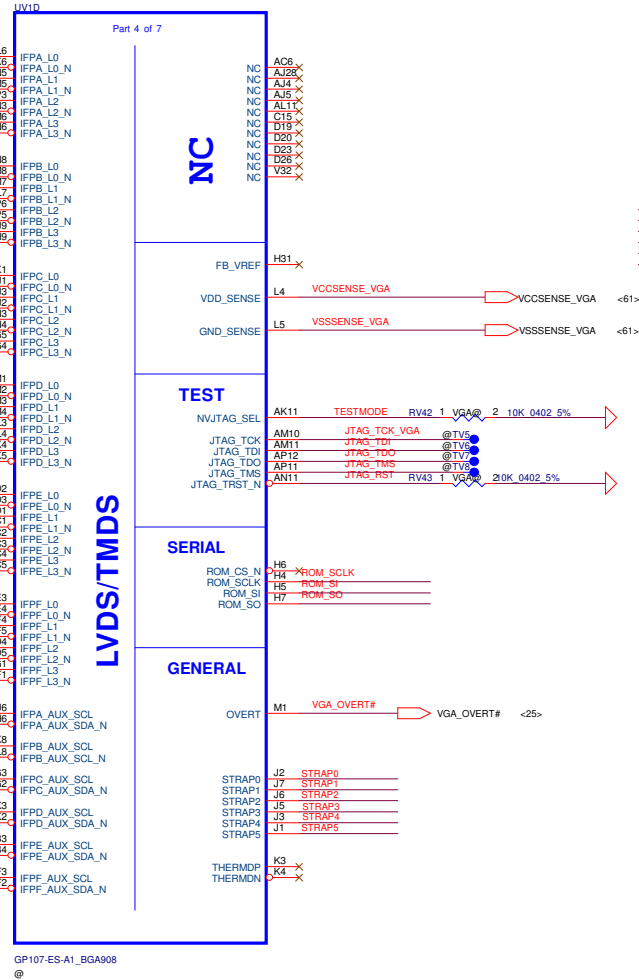
VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

GDDR5 Mode H Mapping

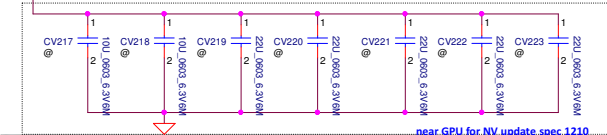
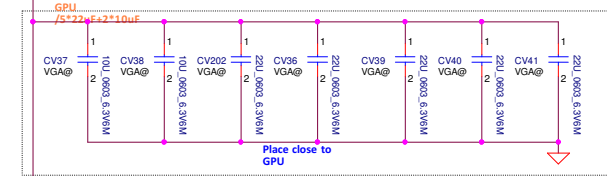
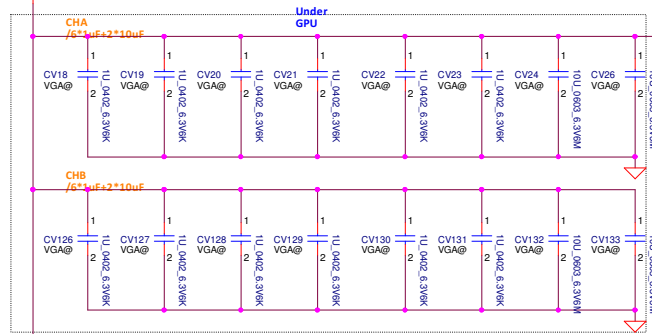


HDMI
2.0

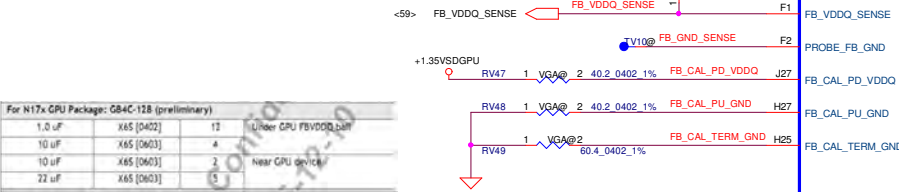
eDP



+1.35VSDGPU



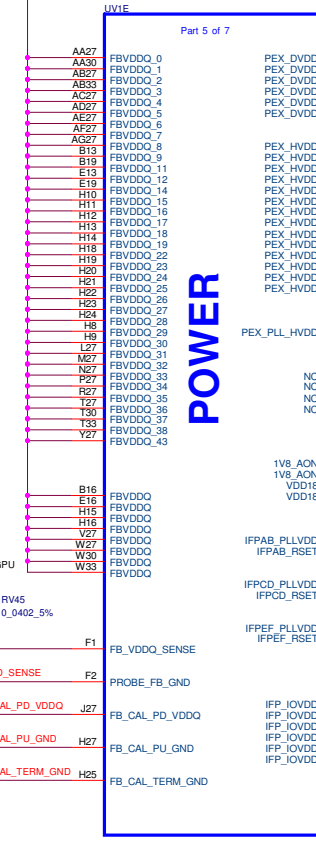
Memory	FBVDDQ	FB_CAL_PU_GND	FB_CAL_PD_VDDQ	FB_CAL_TERM_GND
GDDR5	1.5 V	40.2 Ω	40.2 Ω	60.4 Ω
GDDR5	1.55 V	40.2 Ω	40.2 Ω	60.4 Ω
GDDR5	1.35 V	40.2 Ω	40.2 Ω	60.4 Ω



For H17+ GPU Package: GB4C-128 (preliminary)				
Capacitor Type	Footprint	Population	N16	N17
1.0 μF	X65 [0402]	12	2	4
10 μF	X65 [0603]	4	2	4
10 μF	X65 [0603]	2	2	4
22 μF	X65 [0603]	5	2	4

GPU	Type	Footprint	Population		Location
			N16	N17	
N16P: IFPCD, D, E, F, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z					
N17: IFPCD, PLVDD and IFPE, PLVDD Supply Rails					
GB4C-128	0.1 μF	X75	0402	3	N16P: Under GPU, 1 per ball
GB4C-128	1.0 μF	X65	0402	2	N16P: Under GPU, 1 per ball
GB4C-128	4.7 μF	X5R	0603	1	Near GPU
Bead Type					
L1=300 Ω @ 100 MHz (ESR=0.25 Ω)		0603	1	0	Near GPU

GPU	Type	Footprint	Population	N16	N17	Location
IFPy_IOVDD (N17 IFPy_IOVDD) Supply Rails						
GB4B-128, GB4C-128	0.1 μF	X7R	0402	6	6	Under GPU, 1 per ball
	1.0 μF	X65	0402	2	3	Near GPU
	4.7 μF	X65	0603	2	3	Near GPU
Bead Type						
L1=180 Ω @ 100 MHz (ESR=0.2 Ω)		0603	2	0	0	Near GPU



POWER

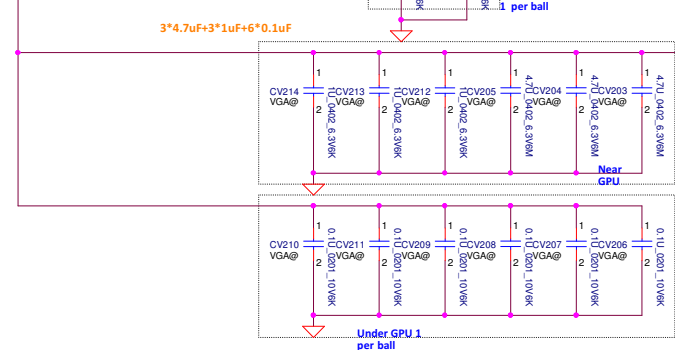
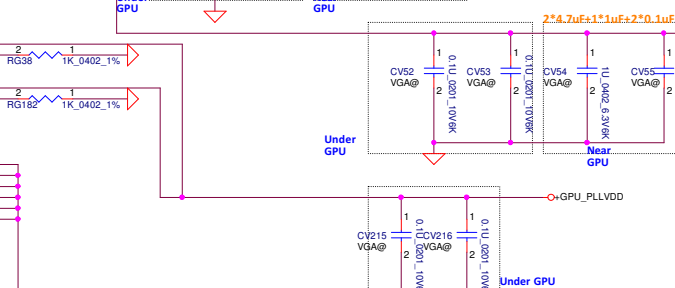
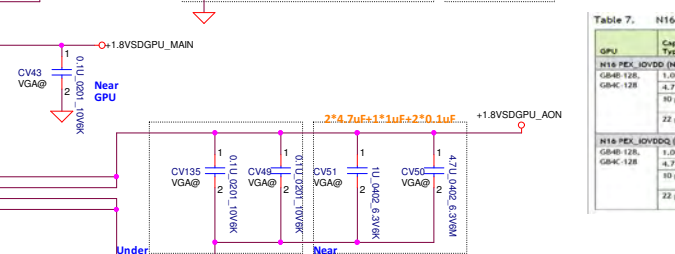
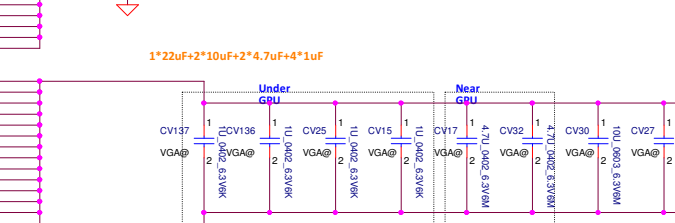
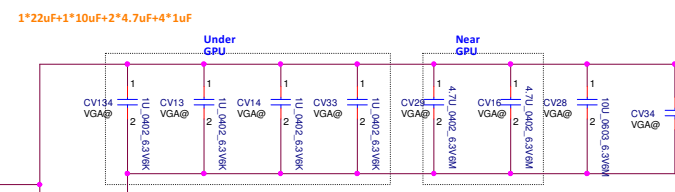
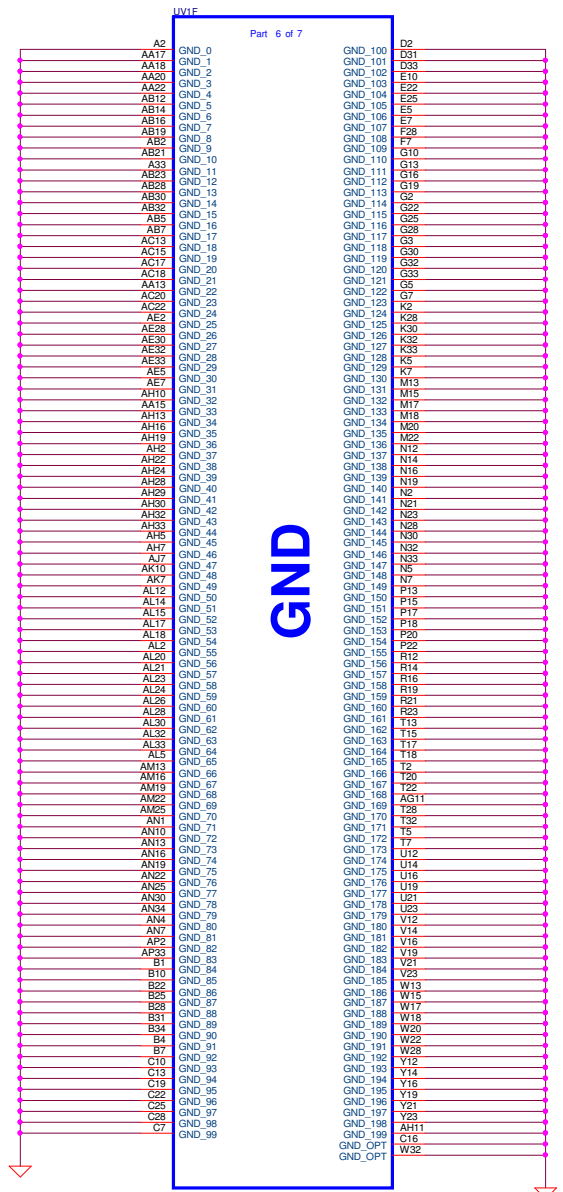
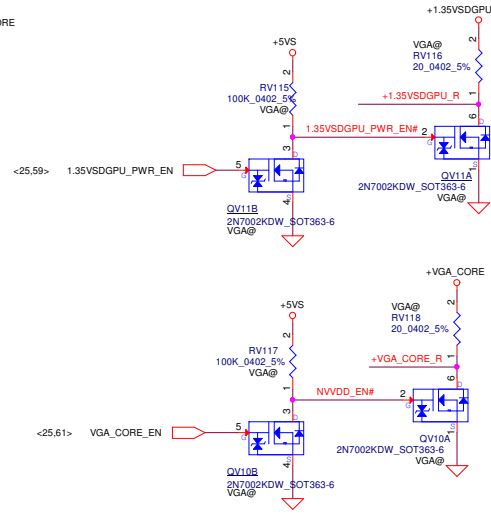
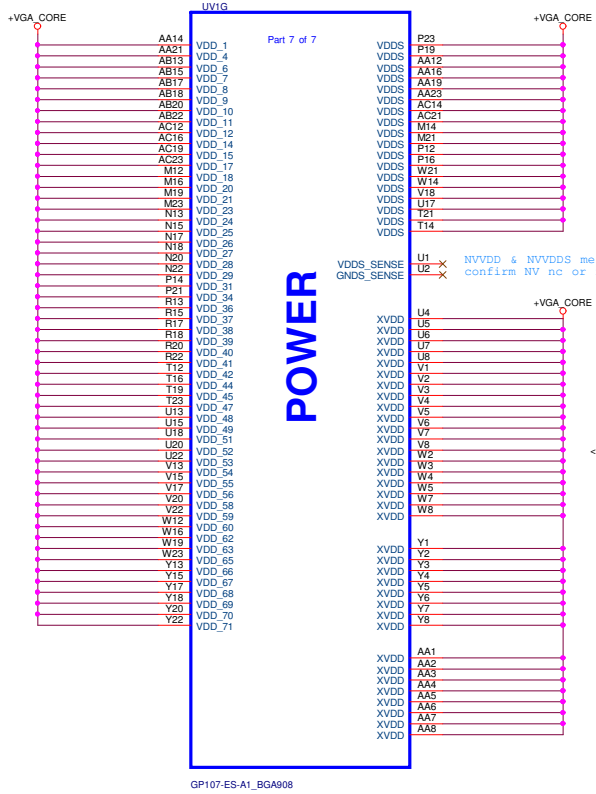
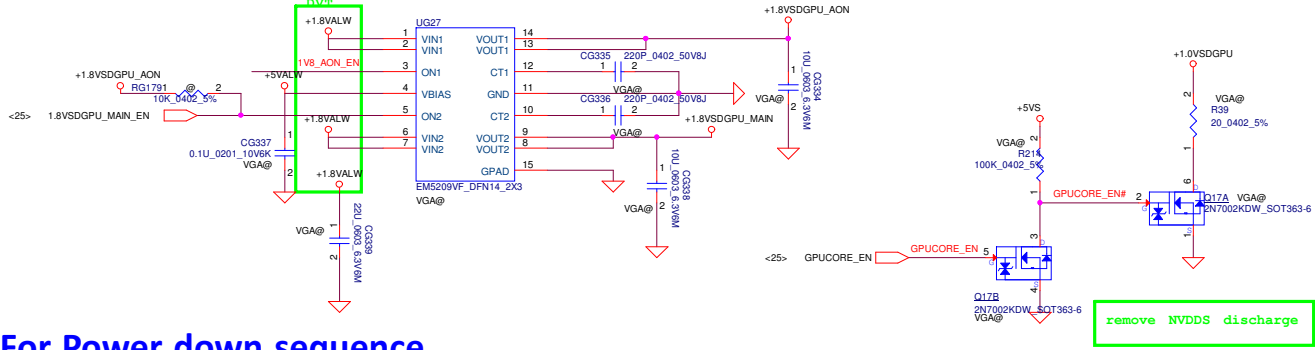


Table 7: N16 and N17 PEX Core and IO Supply Decoupling and Filtering					
GPU	Capacitor Type	Footprint	Population	N16	N17
N16 PEX_IOVDD (N17 PEX_IOVDD) Supply Rails					
GB4C-128	1.0 μF	X65	0402	2	4
GB4C-128	4.7 μF	X65	0603	1	2
	10 μF	X5R	0805	2	1
	22 μF	X5R	0805	2	1
N16 PEX_IOVDD (N17 PEX_IOVDD) Supply Rails					
GB4C-128	1.0 μF	X65	0402	2	4
GB4C-128	4.7 μF	X65	0603	1	2
	10 μF	X5R	0805	2	1
	22 μF	X5R	0805	2	1

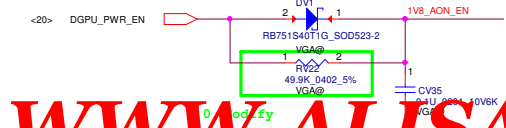
N17P_VDD5
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2



+1.8V_AON/+1.8V_MAIN



For Power down sequence

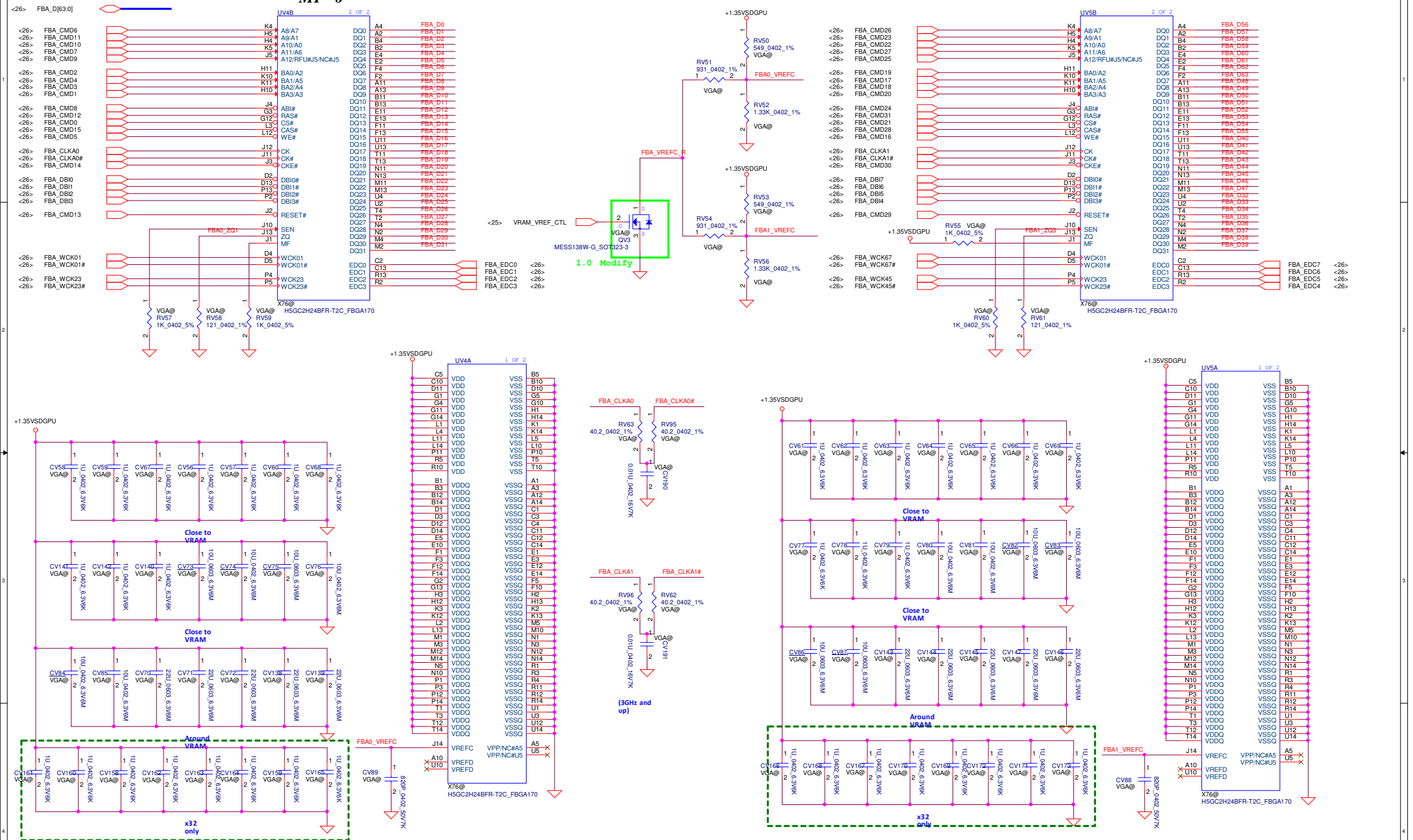


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Size			N17P POWER & GND 5/7
Document Number			DHSVF M/B LA-F591PRO1
Date			Thursday, February 22, 2018
Sheet			29 of 67

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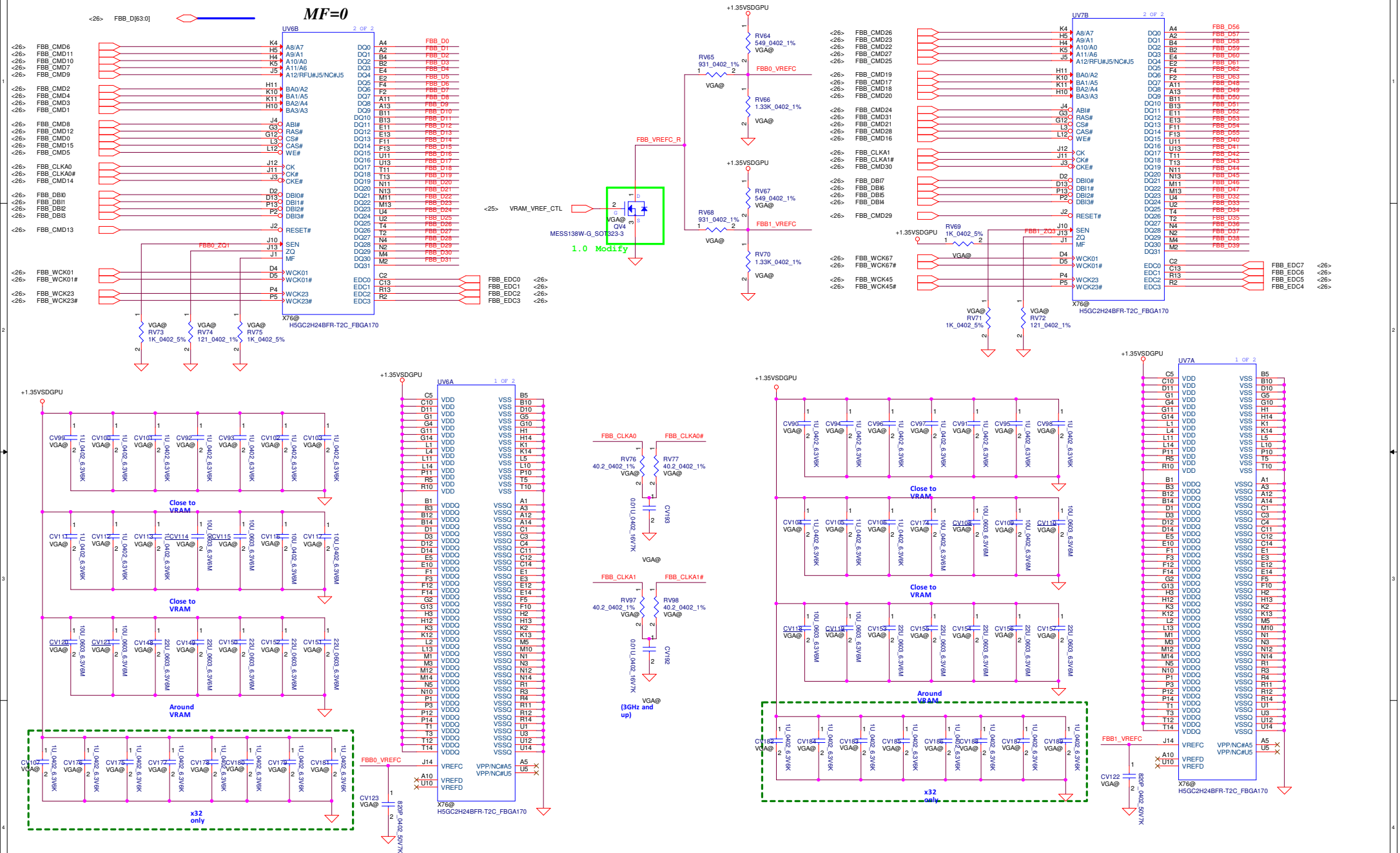


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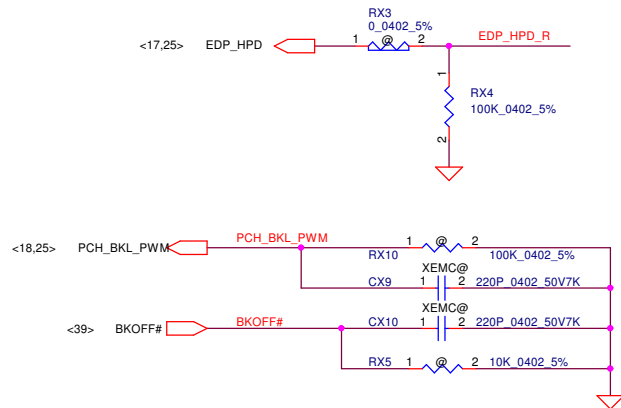
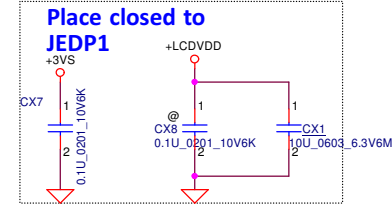
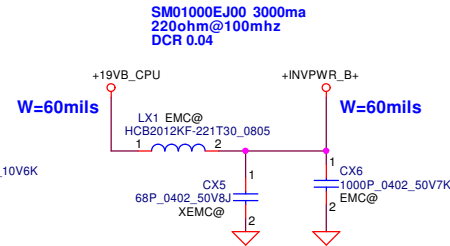
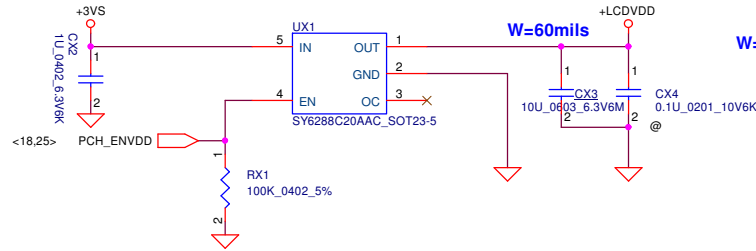
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				Date	Thursday, February 22, 2018
				Sheet	31 of 67

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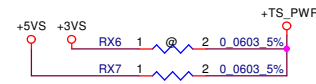
remove GPAK circuit for improve HDMI layout (1.0)

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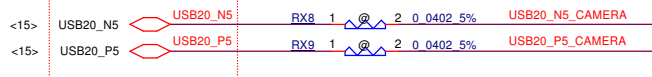
LCD POWER CIRCUIT



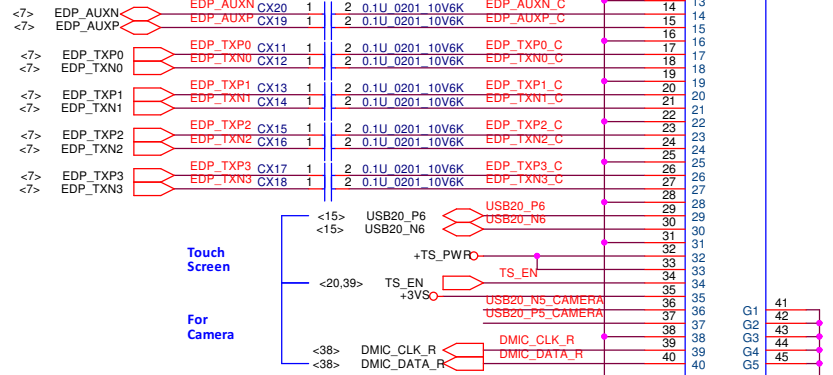
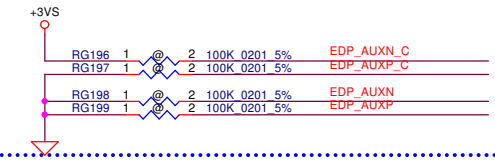
USB Touch Screen



Camera

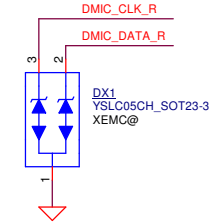


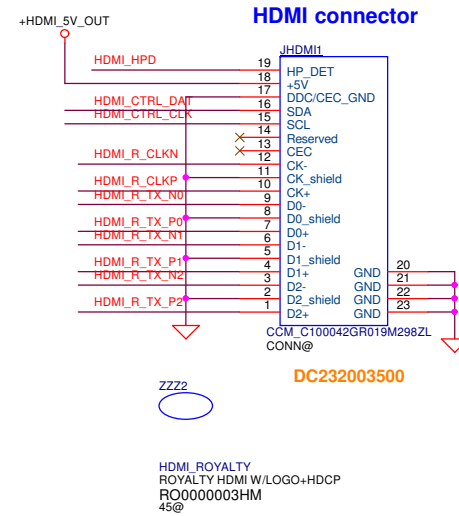
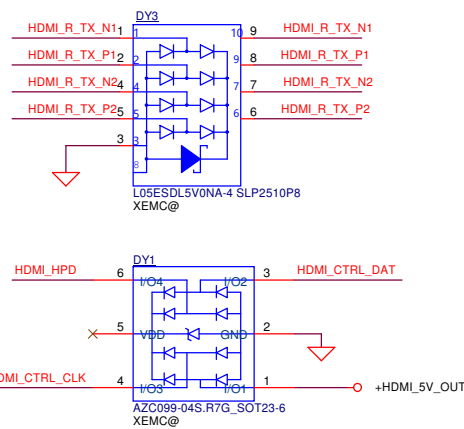
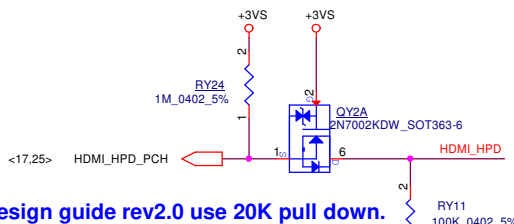
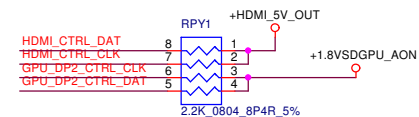
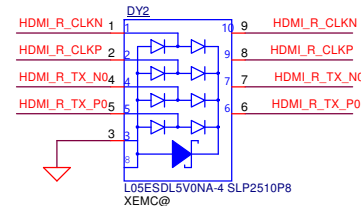
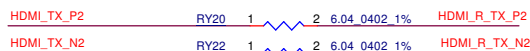
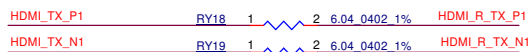
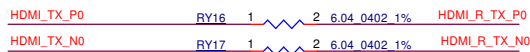
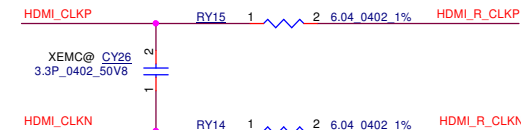
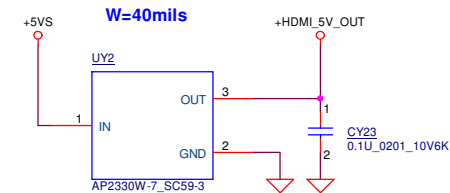
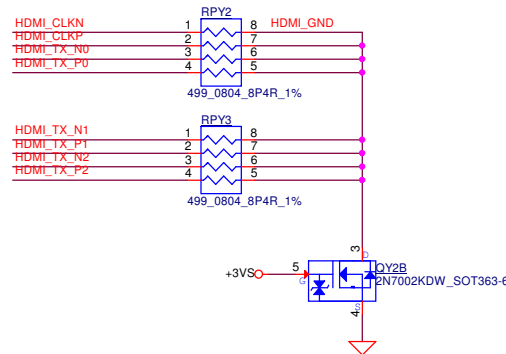
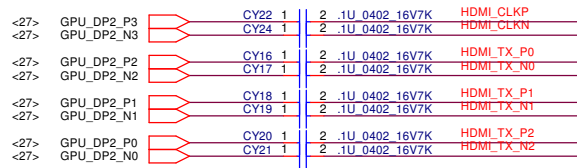
CO-LAY FOR VGA OUTPUT



Touch Screen

For Camera



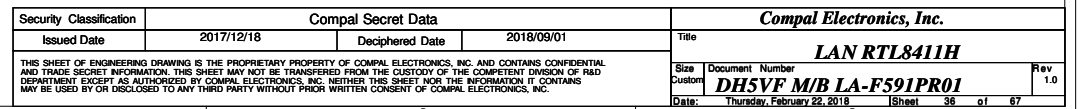


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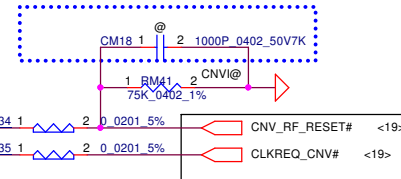
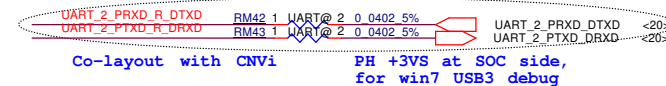
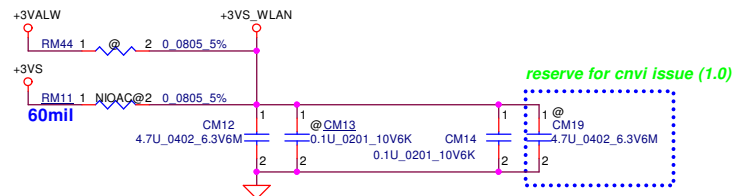
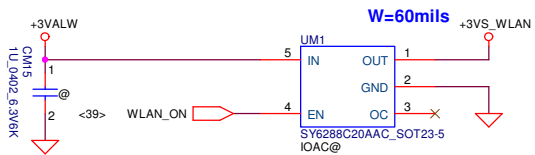
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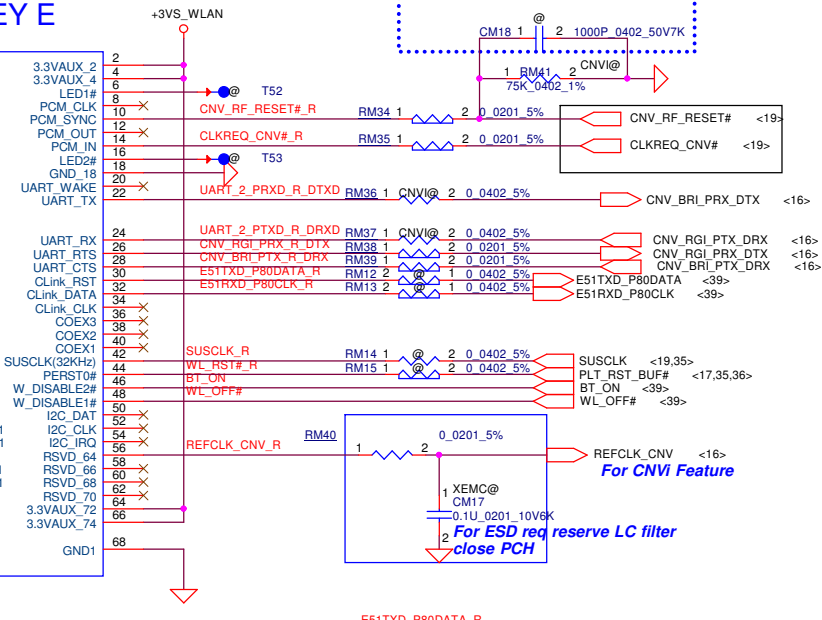
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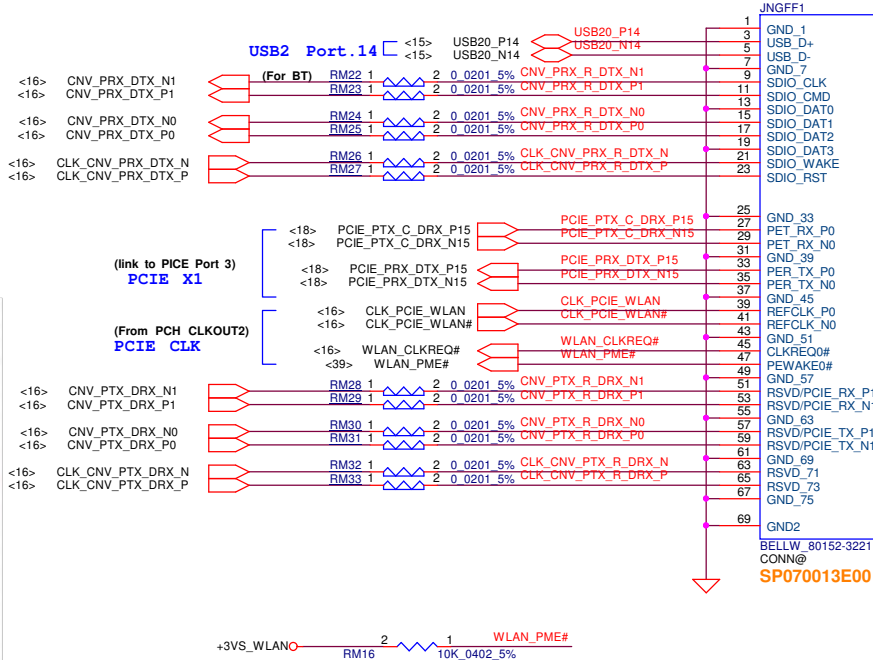
Wireless LAN



KEY E



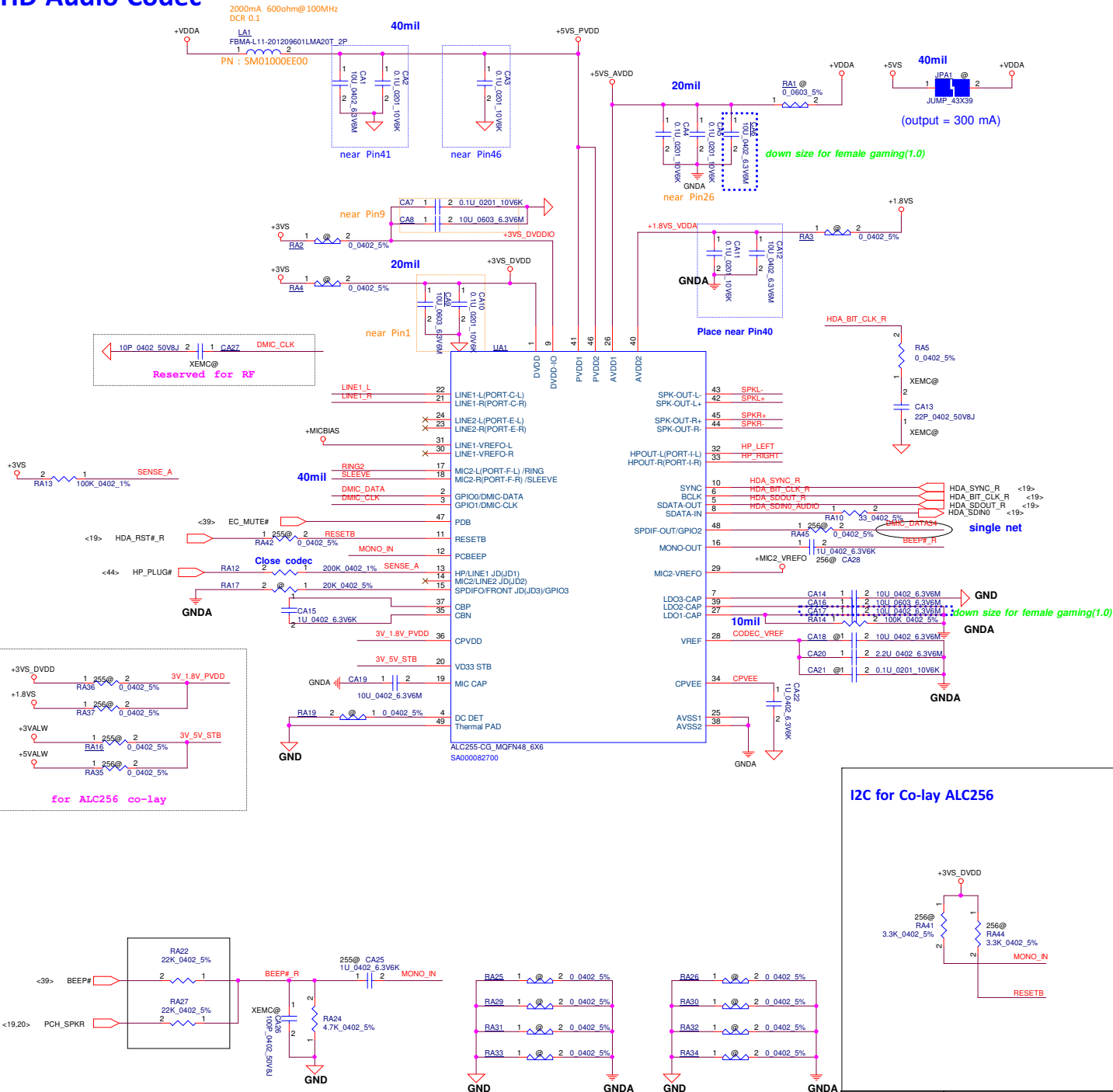
NGFF WL+BT (KEY E)



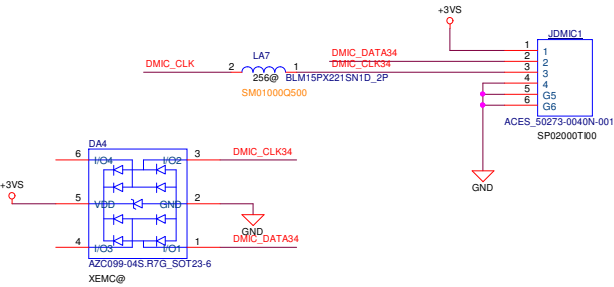
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72	1.0V	RESERVED/REFCLKIN	73
70	UM_Power_SNK/GPIO2/PEWake#	RESERVED/REFCLKP1	71
68	UM_Power_SNK/CLKREQ#	GND	69
66	UM_SWP/PERST#	Reserved/PER#	67
64	RESERVED	Reserved/PERP	65
62	RESERVED	GND	63
60	ALERT# (I/O)(3.3)	Reserved/PETH1	61
58	QDCLK (O)(0/3.3)	Reserved/PETP1	59
56	QD DATA (I/O)(0/3.3)	GND	57
54	W_DISABLE# (O)(0/3.3)	REWake# (O)(0/3.3)	55
52	Reserved/WD_DISABLE# (O)(0/3.3)	CLKREQ# (O)(0/3.3)	53
50	PERSTOR (O)(0/3.3)	GND	51
48	SUSCLK(32kHz) (O)(0/3.3)	REFCLKNO	49
46	CODEK1 (I/O)(0/1.8)	REFCLKPG	47
44	CODEK3 (O)(0/1.8)	GND	45
42	VENDOR DEFINED	PCARD	43
40	VENDOR DEFINED	PEP#	41
38	VENDOR DEFINED	GND	39
36	UART#15 (O)(0/1.8V)	PETNO	37
34	UART#15 (O)(0/1.8V)	PEP#	35
32	UART#1X (O)(0/1.8V)	GND	33
22	UART#6 (I/O)(0/1.8V)	SDIO_Wakeup# (I/O)(0/1.8V)	23
20	UART_Wakeup# (O)(0/3.3V)	SDIO_CLK# (O)(0/1.8V)	21
18	GND	SDIO_DATA# (O)(0/1.8V)	19
16	LED#2 (I/O)(0)	SDIO_DATA# (O)(0/1.8V)	17
14	PCMC_OUT/DS_SD_OUT (O)(0/1.8V)	SDIO_DATA# (O)(0/1.8V)	15
12	PCMC_IN/DS_SD_IN (I/O)(0/1.8V)	SDIO_DATA# (O)(0/1.8V)	13
10	PCMC_SYNC/DS_WS (O)(0/1.8V)	SDIO_CMD# (O)(0/1.8V)	11
8	PCMC_CLK/DS_SCK (O)(0/1.8V)	SDIO_CLK# (O)(0/1.8V)	9
6	LED#1 (I/O)(0)	GND	7
2	USB_	USB_	3
		GND	4

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Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	M.2 Key E (WLAN)	
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				Custom	DH5VF M/B LA-F591PR01	1.0
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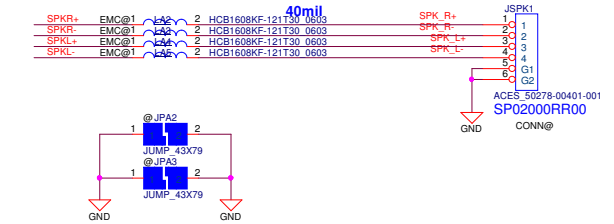
HD Audio Codec



DMIC3 Conn. (support on 256)

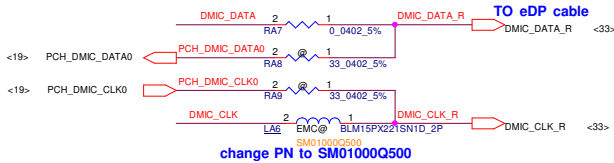


Int. Speaker Conn.

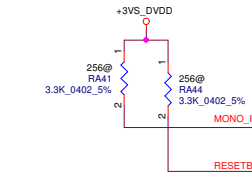


Digital MIC

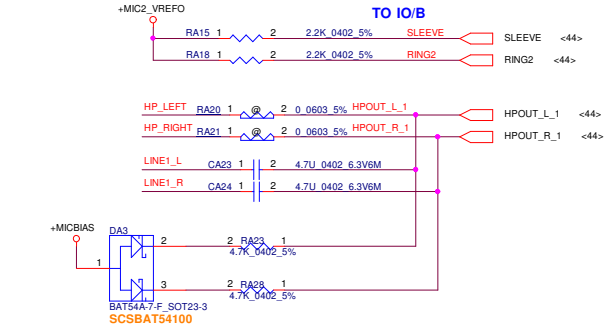
MIC BOM upload by Audio Team



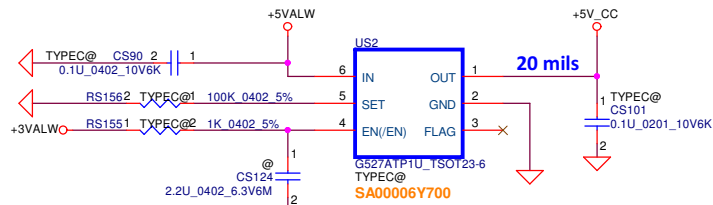
I2C for Co-lay ALC256



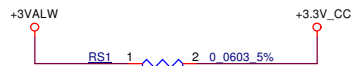
Headphone Out



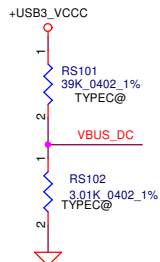
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/12/18	Deciphered Date	2018/09/01	Title	
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0.2A OCP for VCONN!



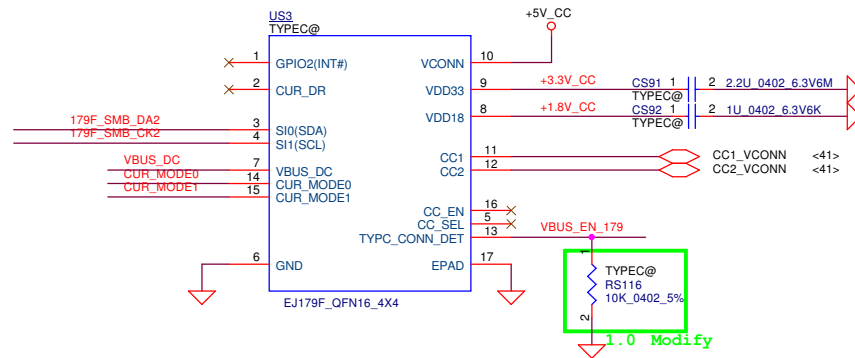
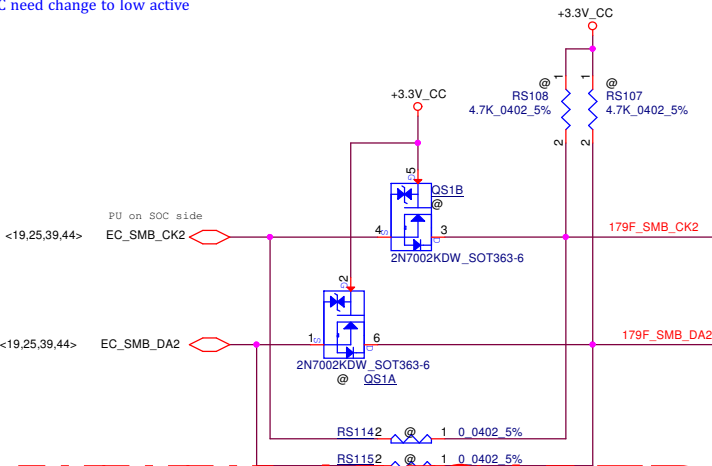
1.0 Modify



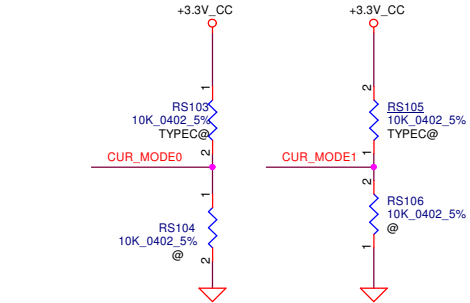
Scaled input
for detection of VBUS DC levels

Remove INI#,
platform doesn't monitor it
report CC1 or CC2 is connection
CC_EN
power path control "low active"

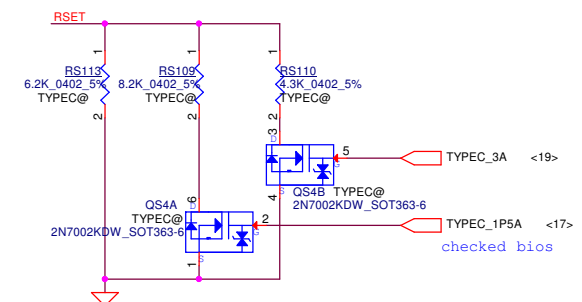
EC need change to low active



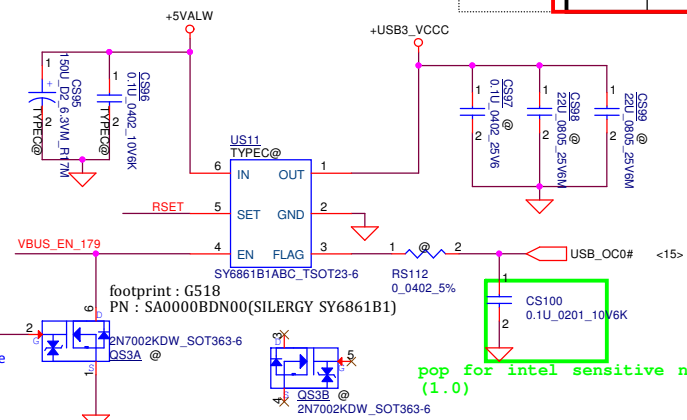
1.0 Modify



Initial Current mode selection		
CUR_MODE0	CUR_MODE1	MODE
H	L	Default Current
L	H	Medium current
H	H	High current



G518 MOS Current Limit				
GPP_B1 (TYPEC_3A)	GPP_B4 (TYPEC_1P5A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
H	H	1.94	3A	3.5A



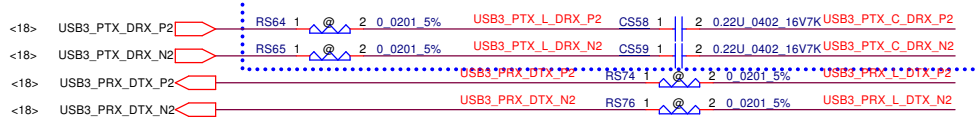
EC need change to low active

pop for intel sensitive net
(1.0)

Initial Current mode selection		
VBUS_EN_179	EC_TYPEC_EN#	V BUS
L	H	0
L	L	0
H	H	0
H	L	1

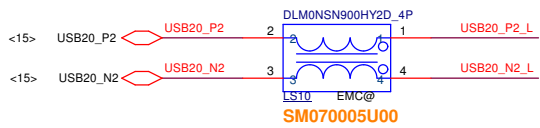
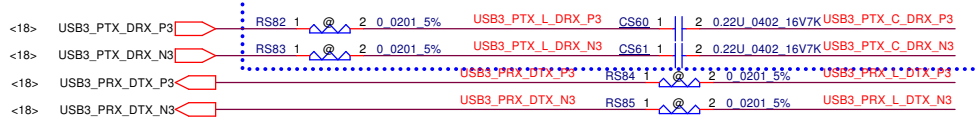
USB3.0 (Port 3)

Change to 0201 for placement. 1A modify

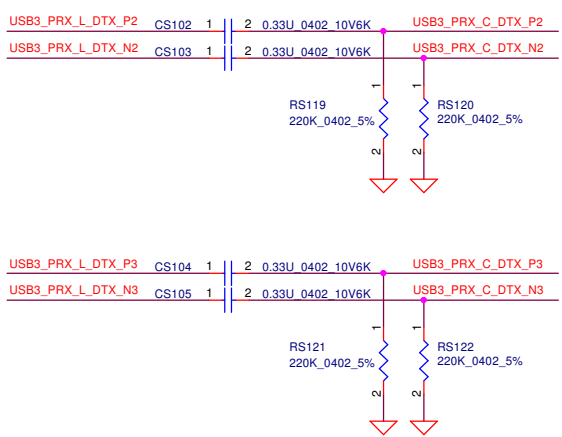


USB3.0 (Port 4)

1A modify

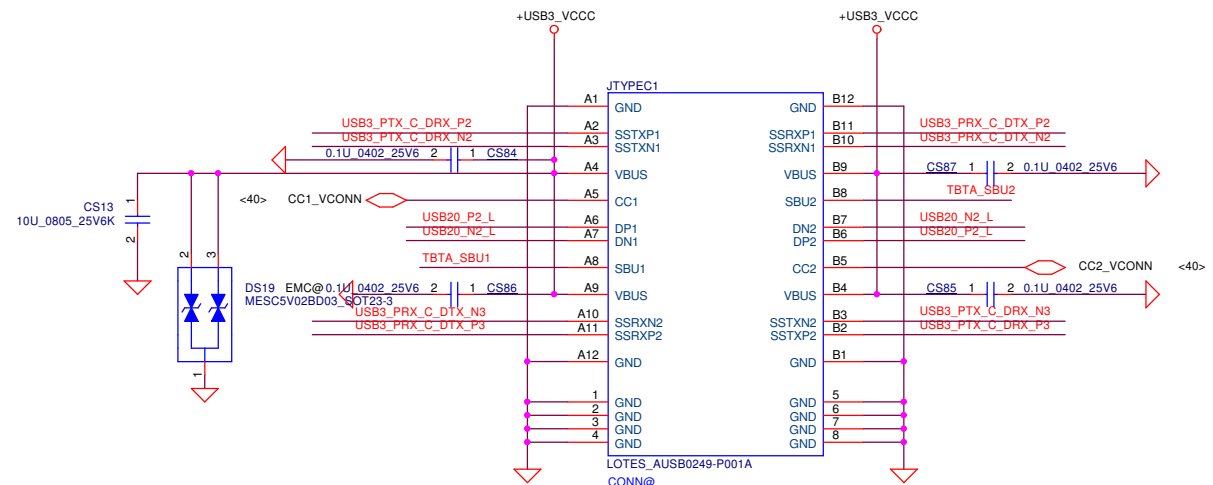
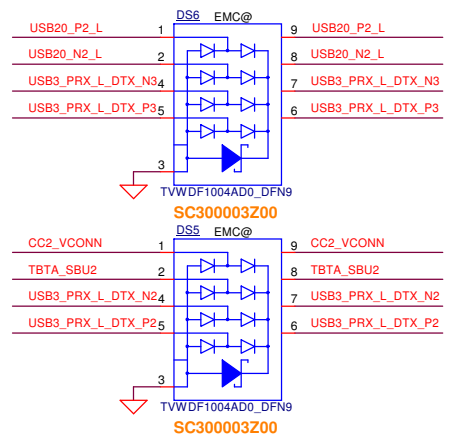
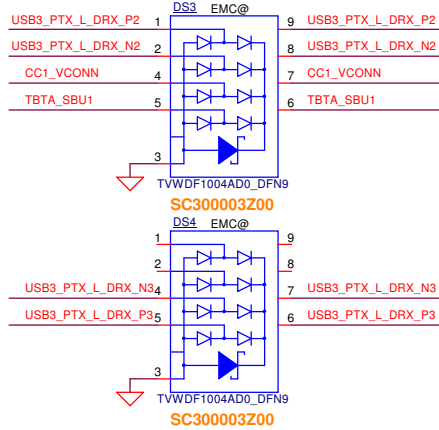


add topology for intel ECN_Update (1.0)



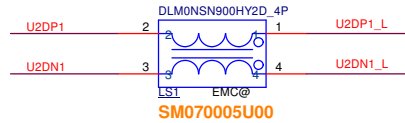
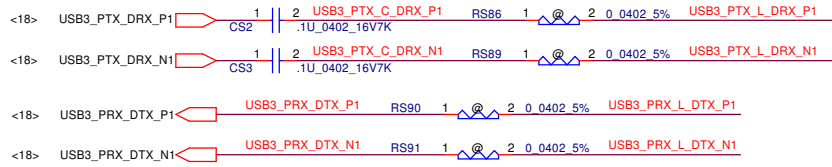
Follow intel #575549 for ESD/EOS protection.

For ESD request

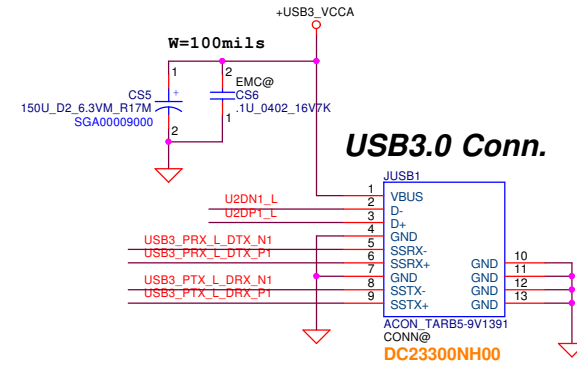
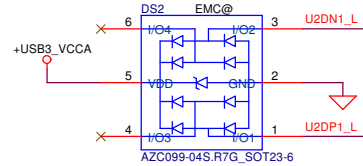
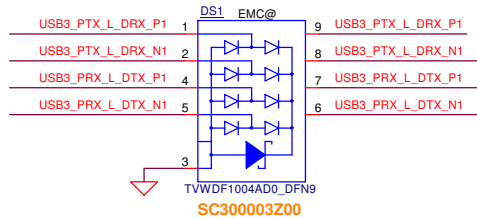


CC1_VCONN & CC2_VCONN need 20mil trace width.

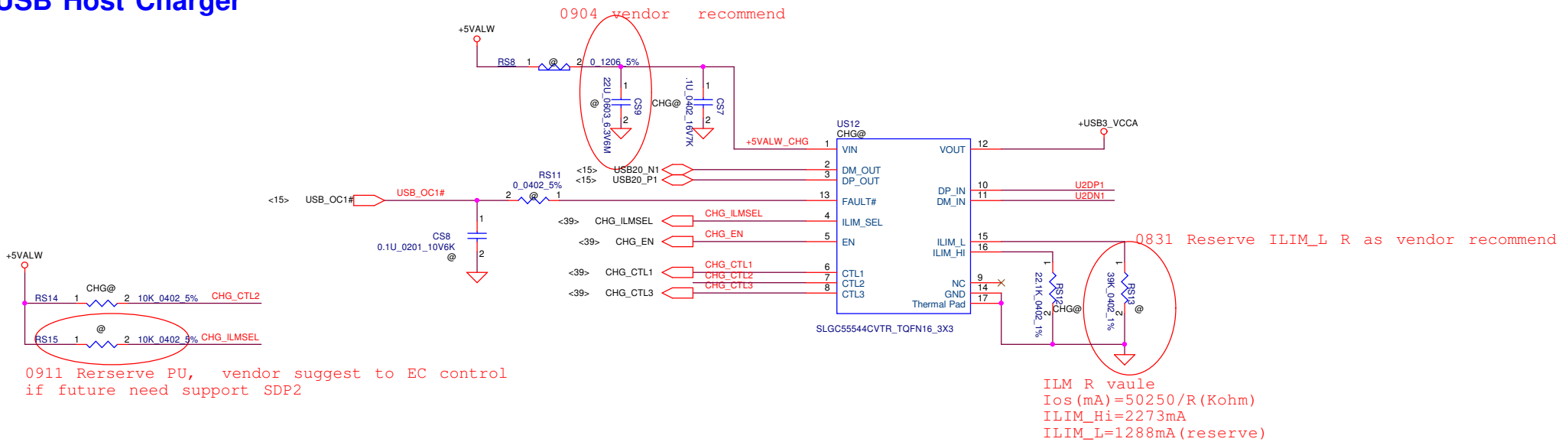
USB3.0 /2.0 CMC



ESD request



USB Host Charger

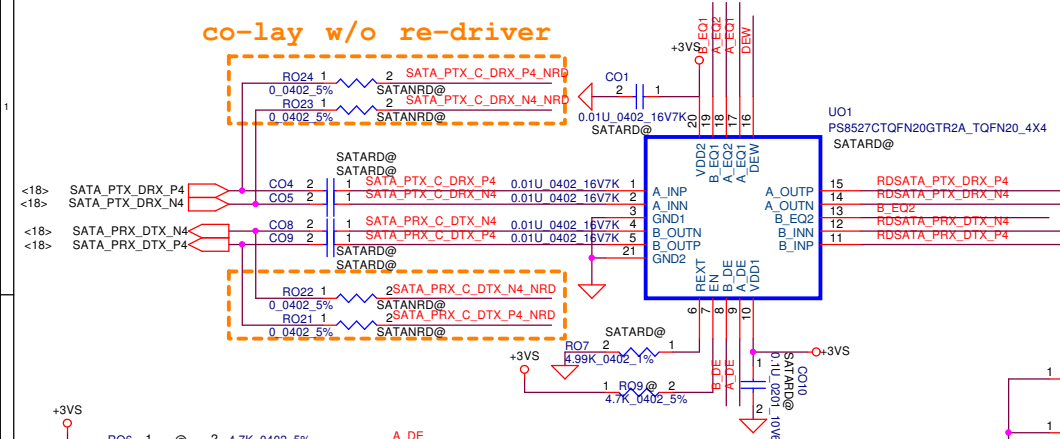


USB Host Charger Truth Table

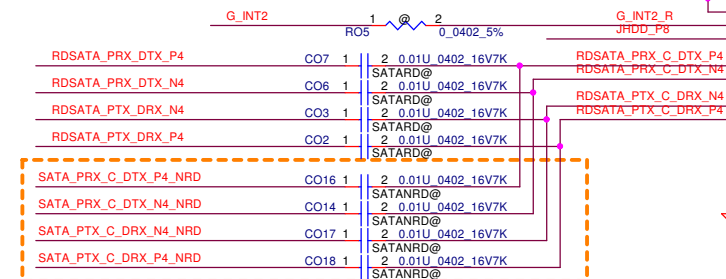
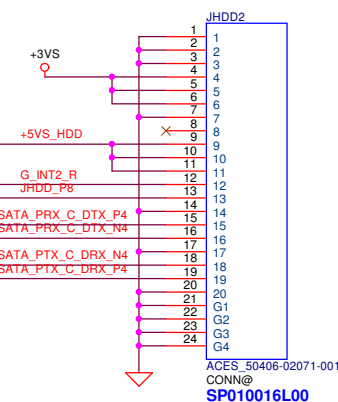
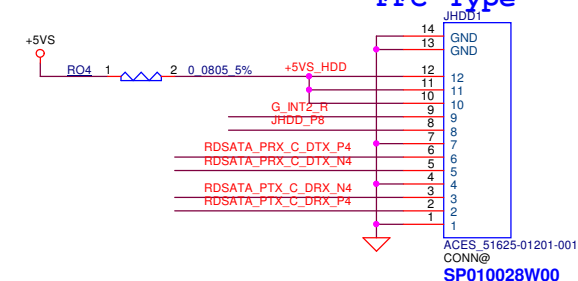
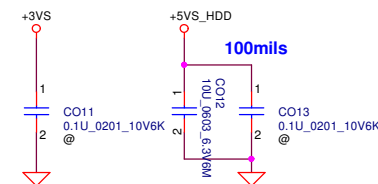
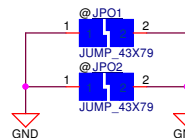
CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	SDP	ILIM_H	Data Lines Connected

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Deciphered Date				2018/09/01				USB3.0 Conn/USB Charger			
Size				Document Number				Rev			
Custom				DHSVF M/B LA-F591PR01				1.0			
Date:				Thursday, February 22, 2018				Sheet 42 of 67			

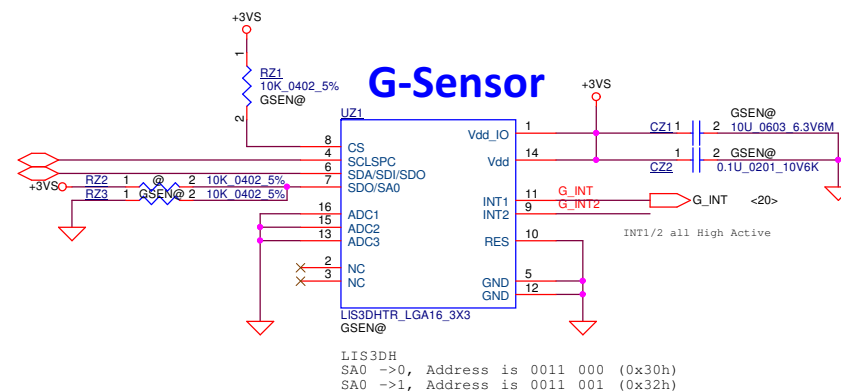
SATA Re-Driver and cable HDD Conn.



USE 8527 re-driver
SA00007JU10



co-lay w/o re-driver



Programmable output de-emphasis level setting for channel A.
Internally tied to VDD/2(M status).

A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Programmable output de-emphasis level setting for channel B.
Internally tied to VDD/2(M status).

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

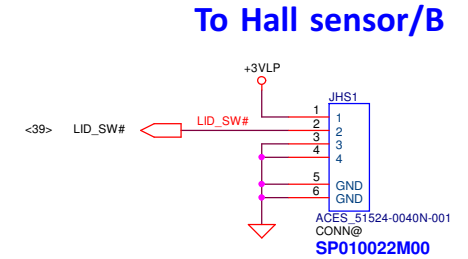
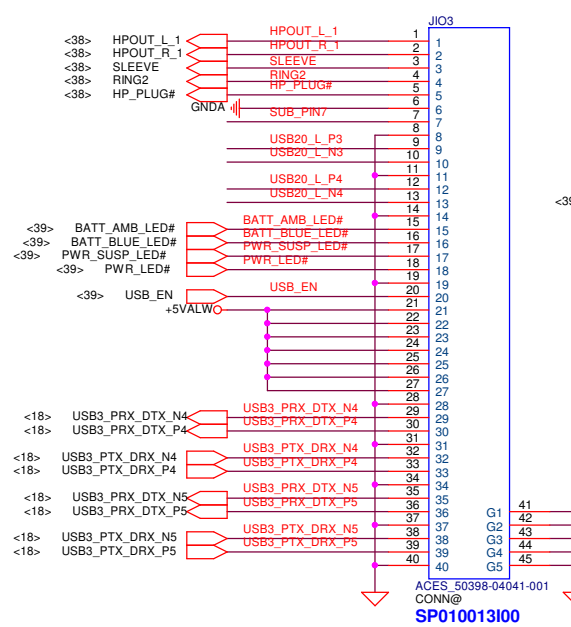
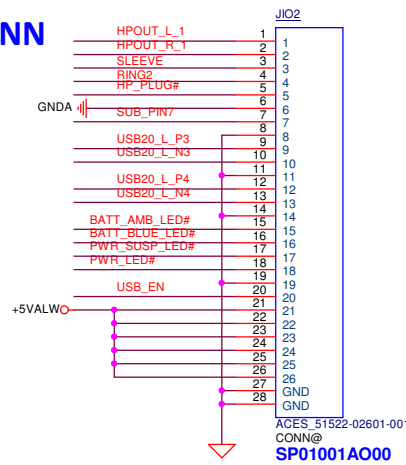
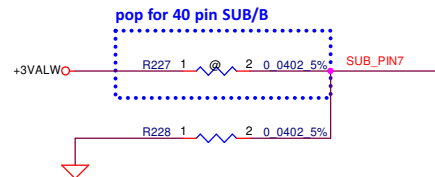
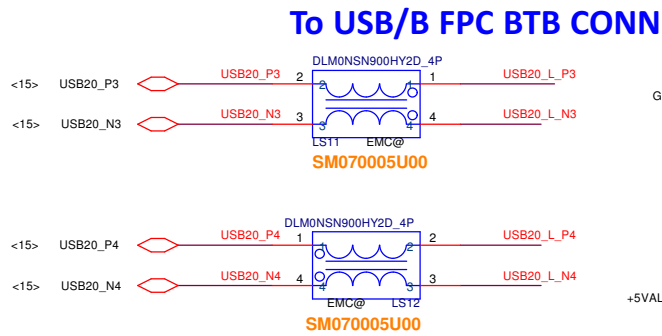
Equalizer control and program for channel A.
Internally tied to VDD/2 (M status).

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

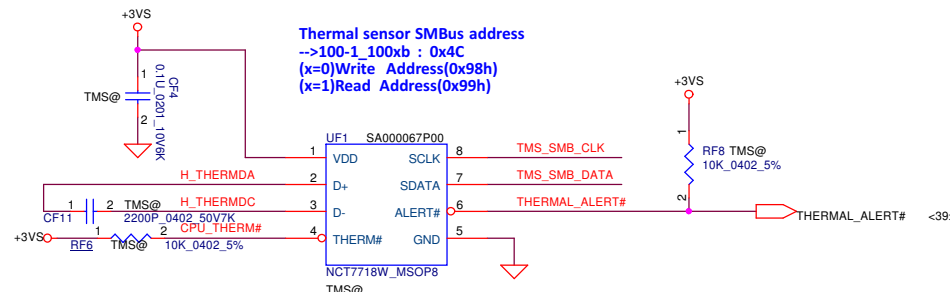
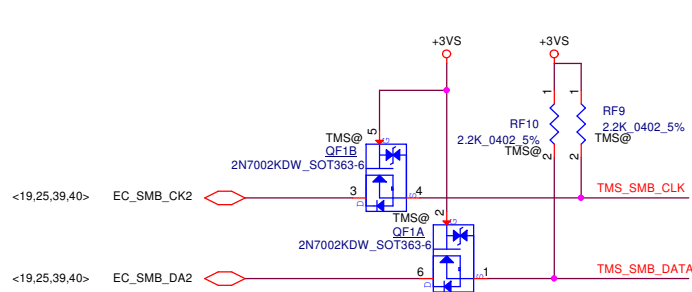
Equalizer control and program for channel B.
Internally tied to VDD/2(M status).

B_EQ2	B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

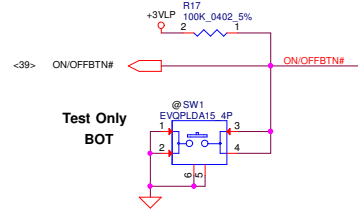
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				Size	Document Number	Rev
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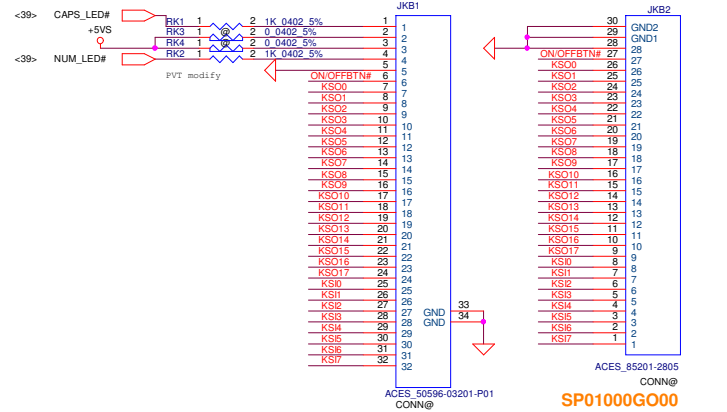
THERMAL SENSOR



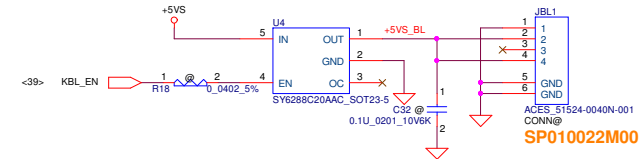
ON/OFF BTN



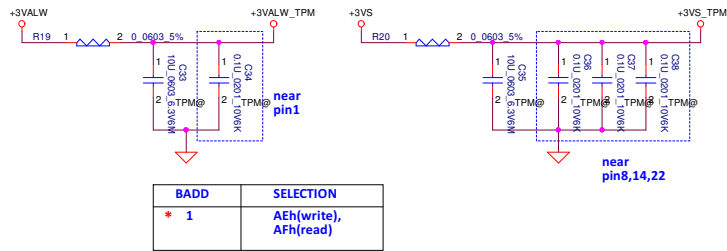
KB Conn.



KB BackLight

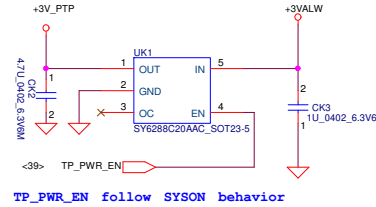


TPM

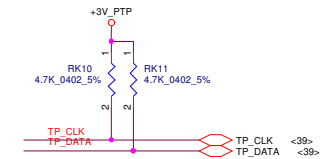
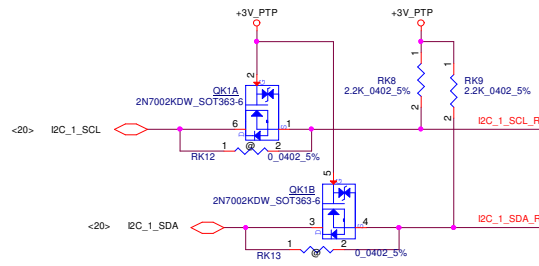
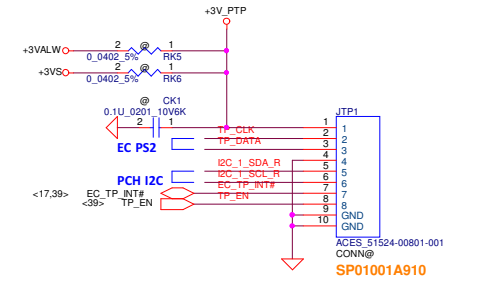


BADD	SELECTION
* 1	Aeh(write), Afh(read)

Touch Pad

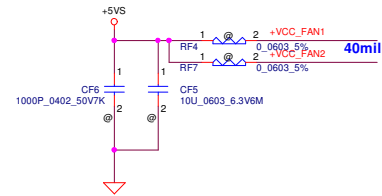


TP_PWR_EN follow SYSON behavior

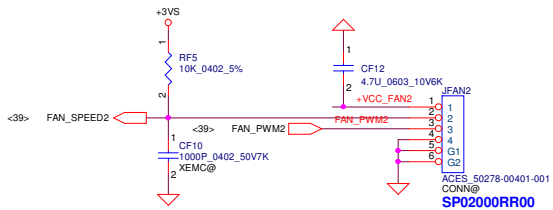
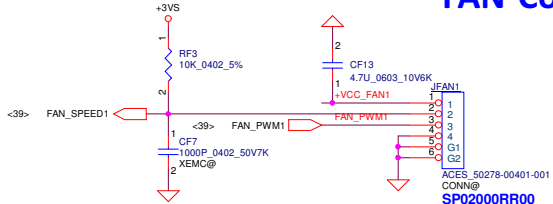


SERIRQ PH 10K to +3VS at PCH side
CLKRUN# PH 10K to +3VS at PCH side
LPCPD# had internal PH

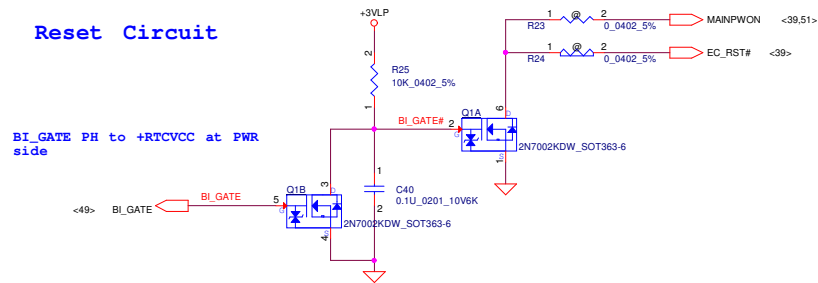




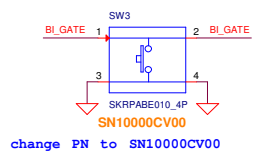
FAN Conn



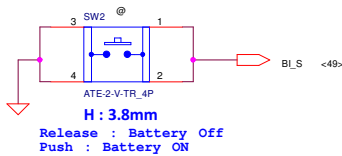
Reset Circuit



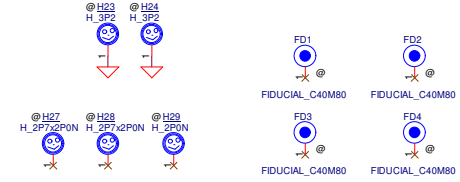
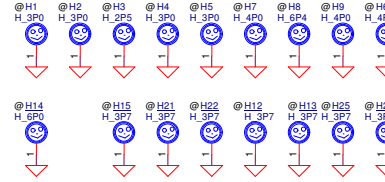
Reset Button



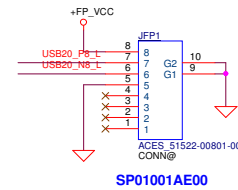
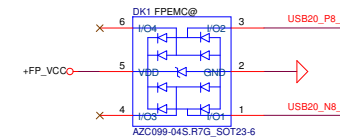
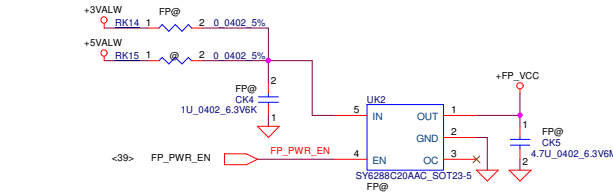
BI SW



Screw Hole



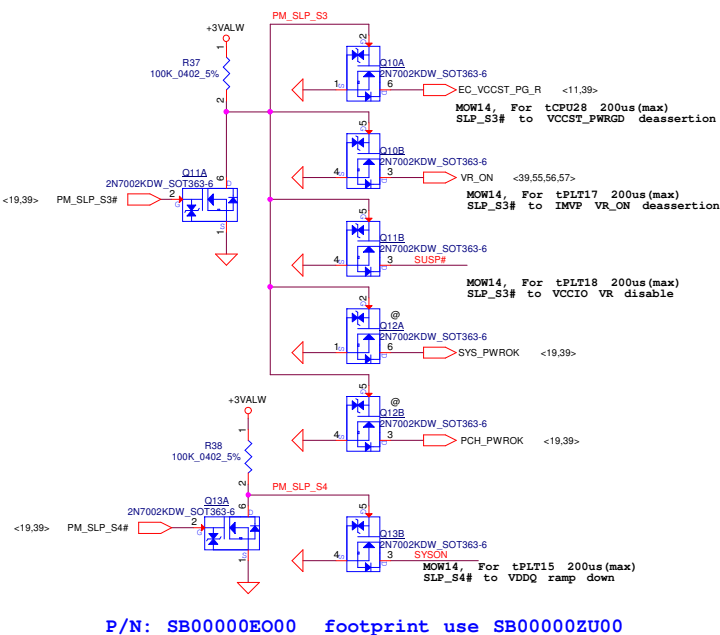
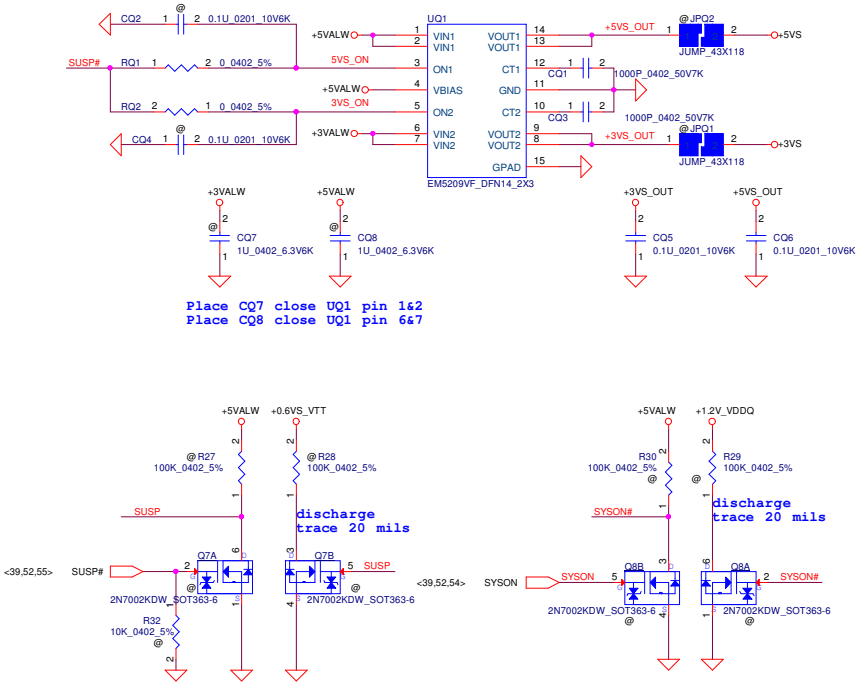
Finger Print



PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

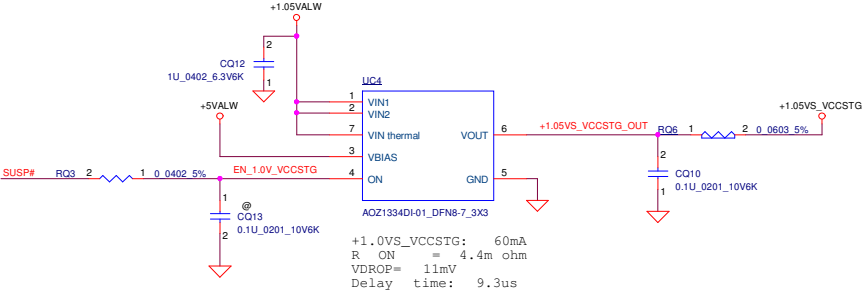
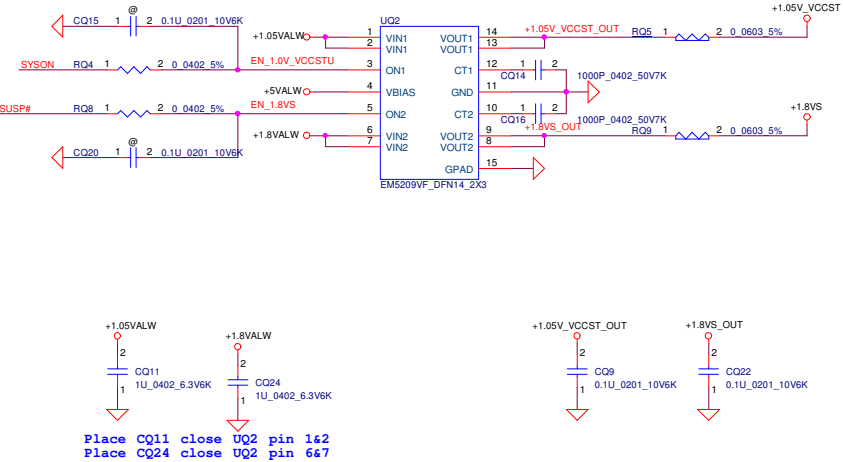
System DC interface

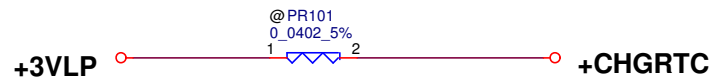
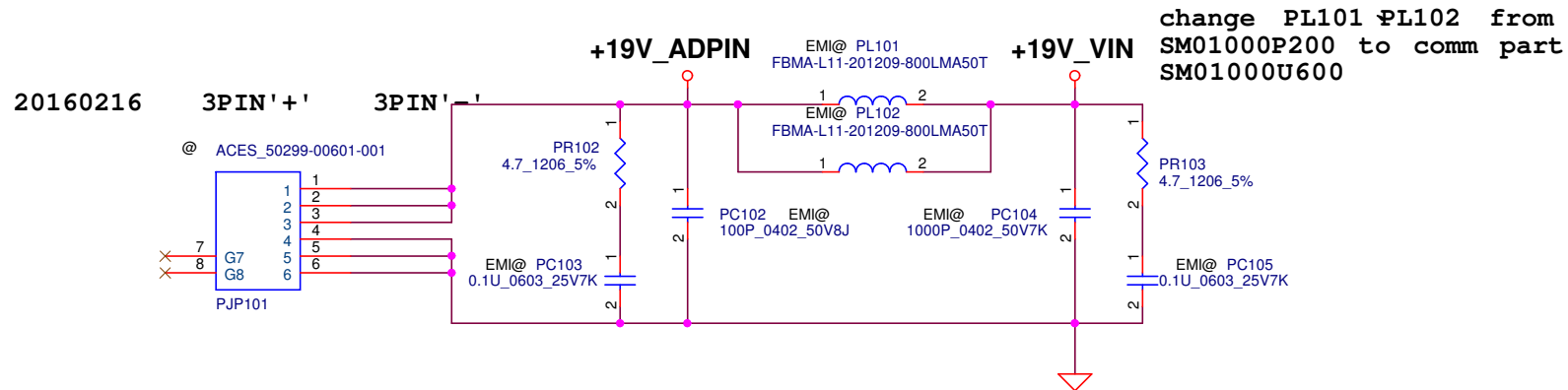
For Power ON/Off Sequence



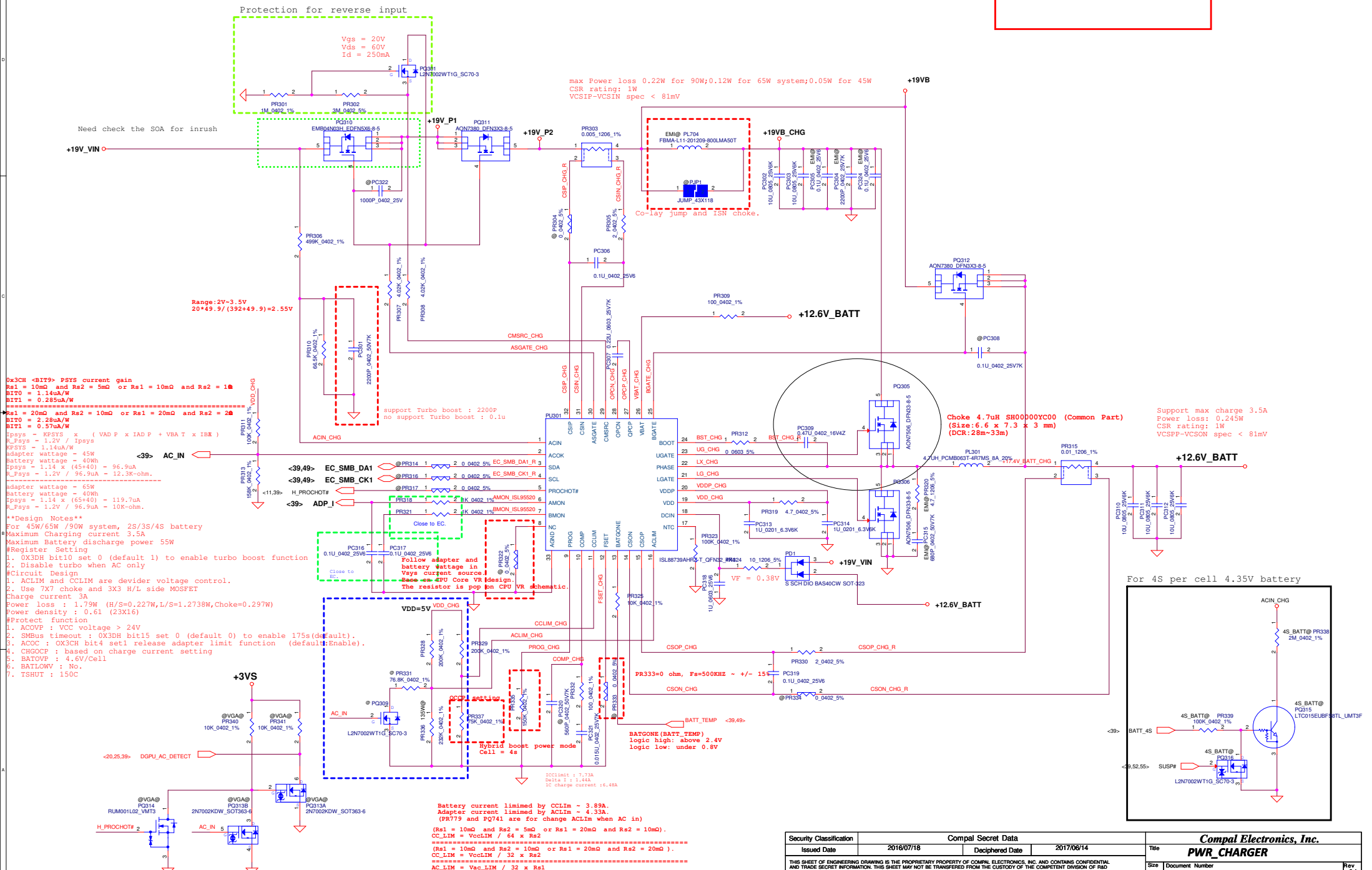
+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS

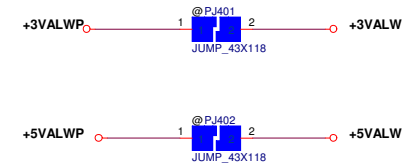
+1.05VALW TO +1.05VS_VCCSTG



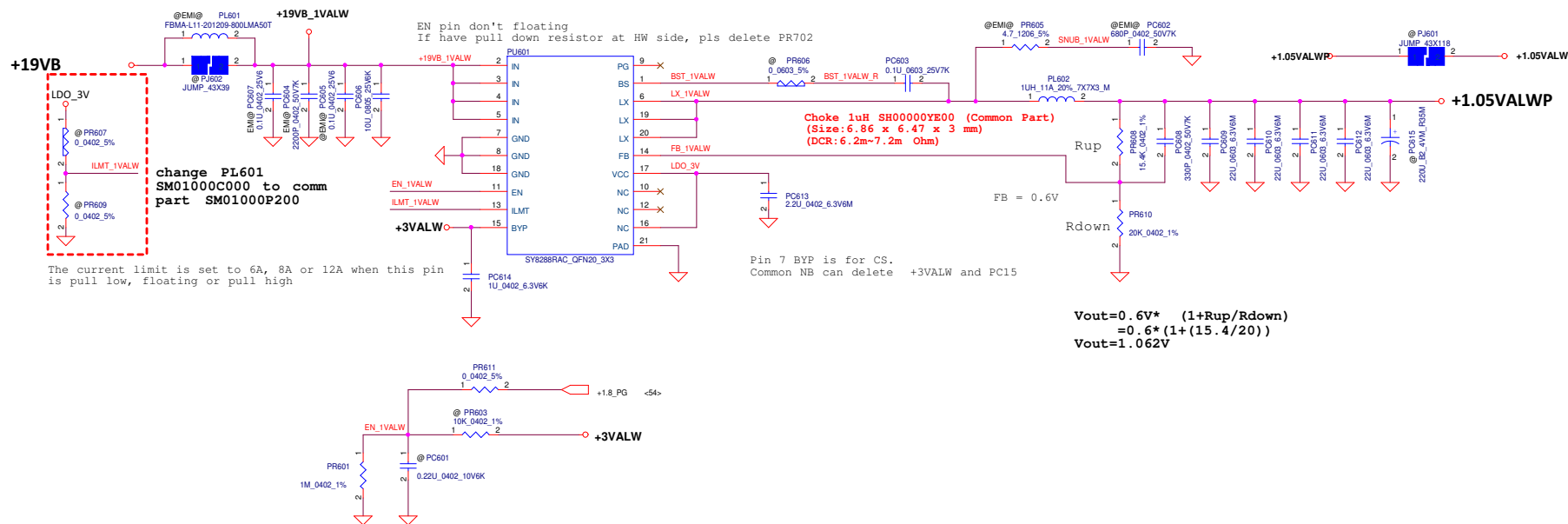


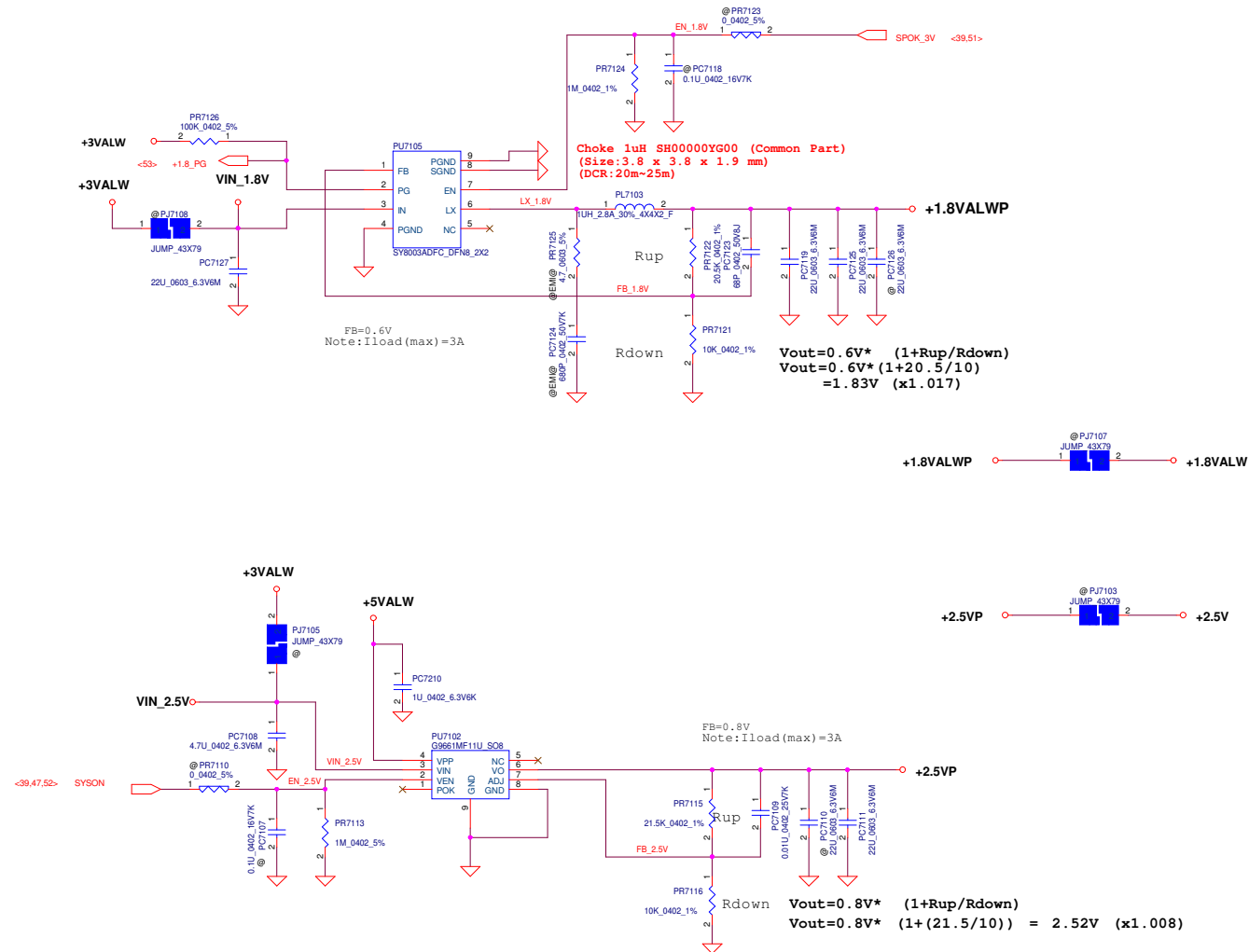
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SET1 connect to 5V is into test mode.
The output is 1.05V.

Local sense, for debug only.
Trace is form output cap that is near choke.

VCCSENSE and VSSSENSE need have
a 100ohm at HW Side

Confirm HW side.
Don't double pull high.

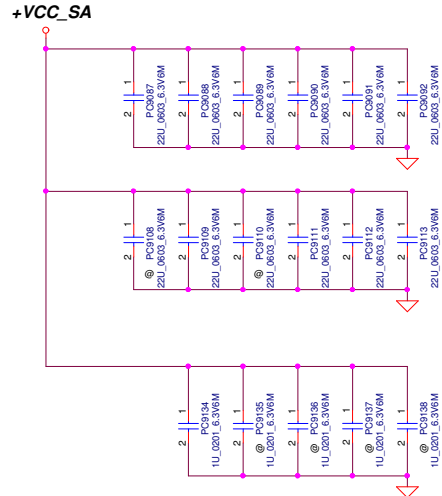
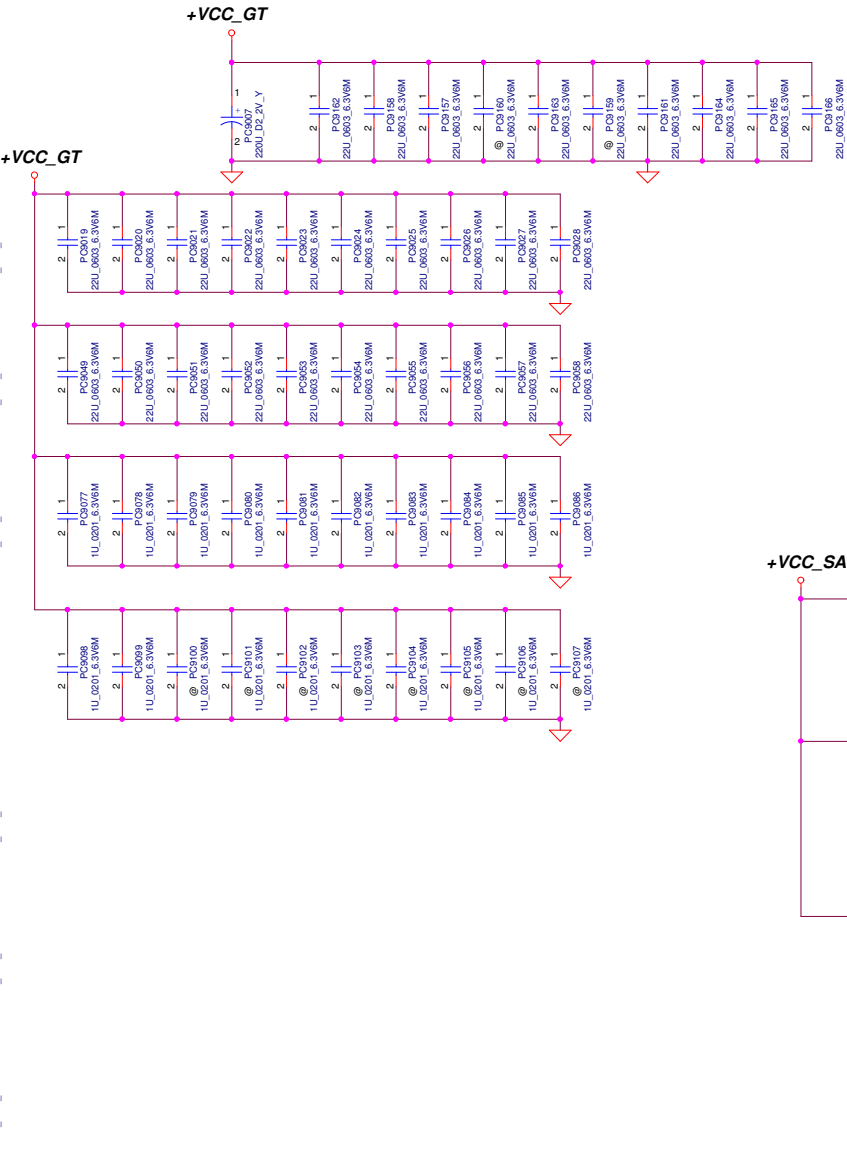
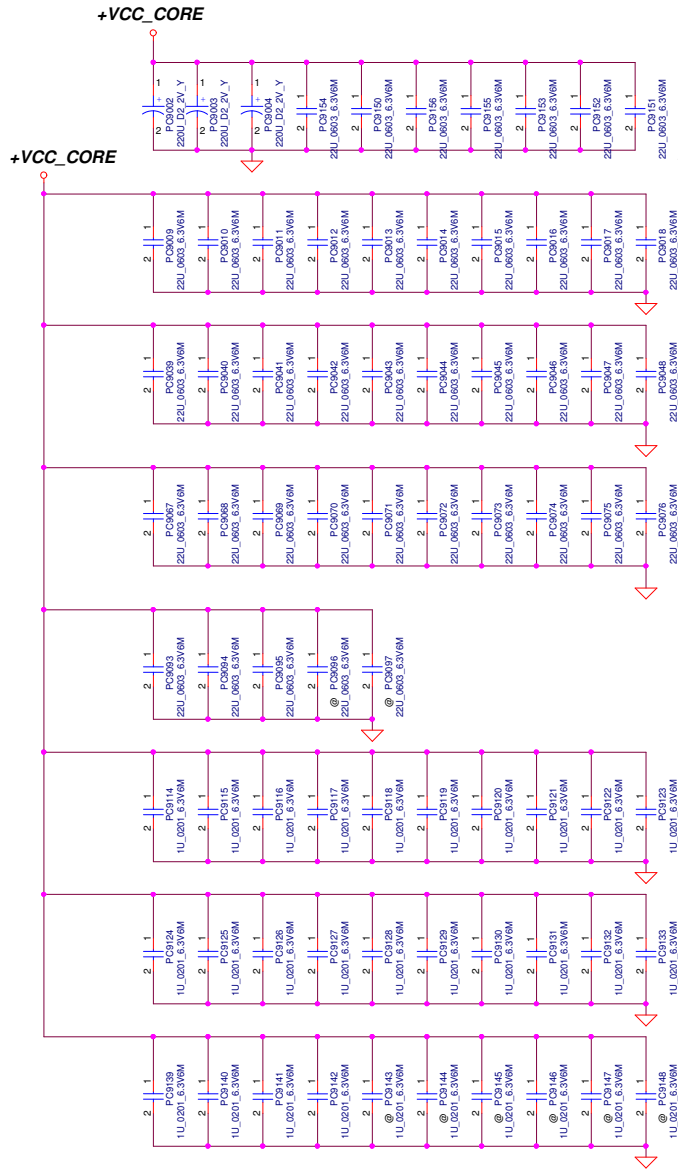
Confirm HW side.
Don't double pull high.

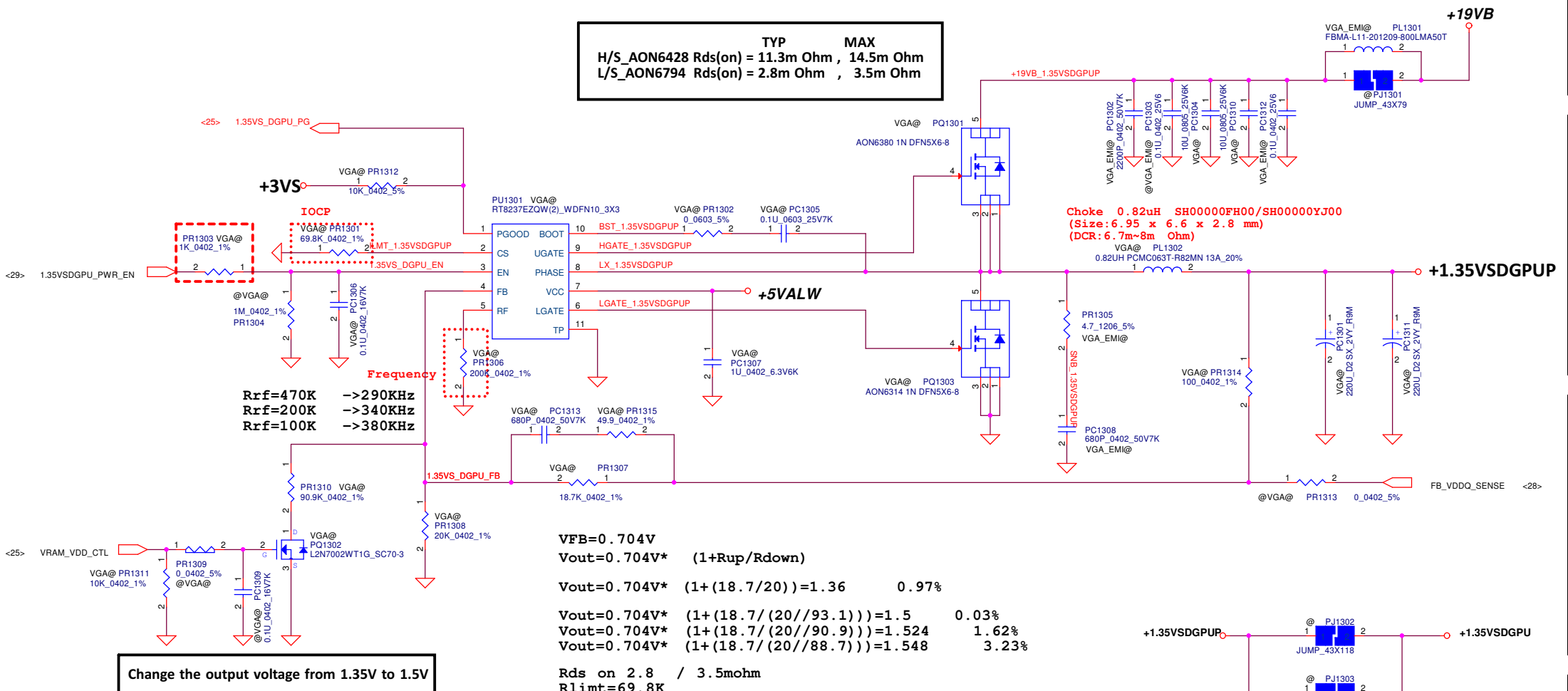
PR902 and PR904 pull high resistor are pop at the end of VR SVID.
Other VR is unpop.
SVID_ALERT# pull high resistor is at HW side.

confirm with power sequence,
it need behind +5VS.

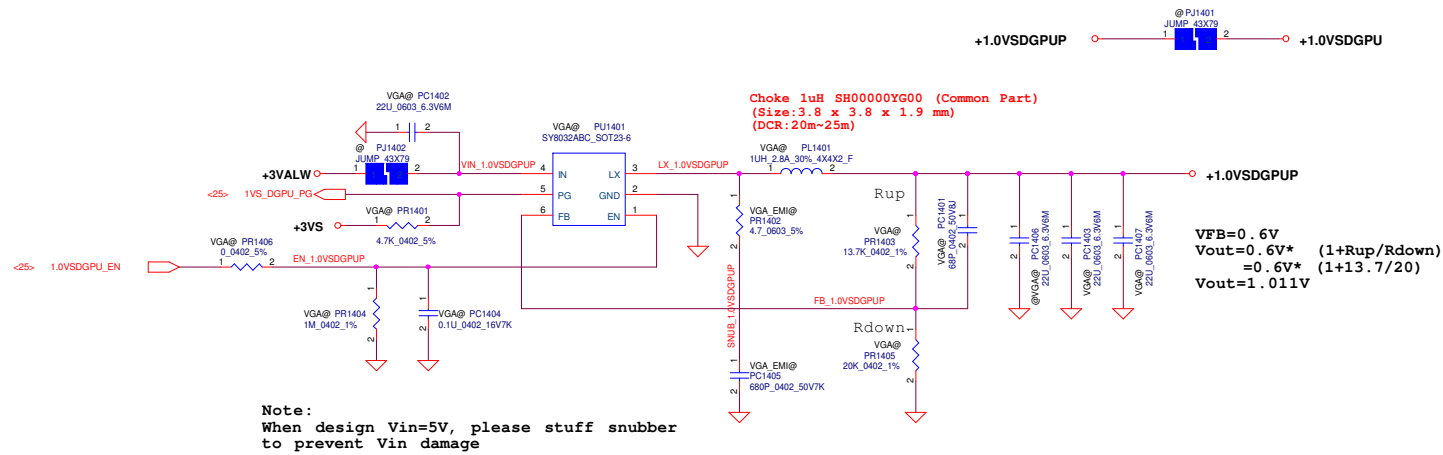
Choke	Size and DCR	7x7x4	7x7x3
IMON		68.1K	73.2K
COMP		10K	1.1K
ISEN		40.2K	37.4K
		604	665
		243	549
		10K	1K
		10K (3370K)	1K (3650K)

For NTC trace routing only.





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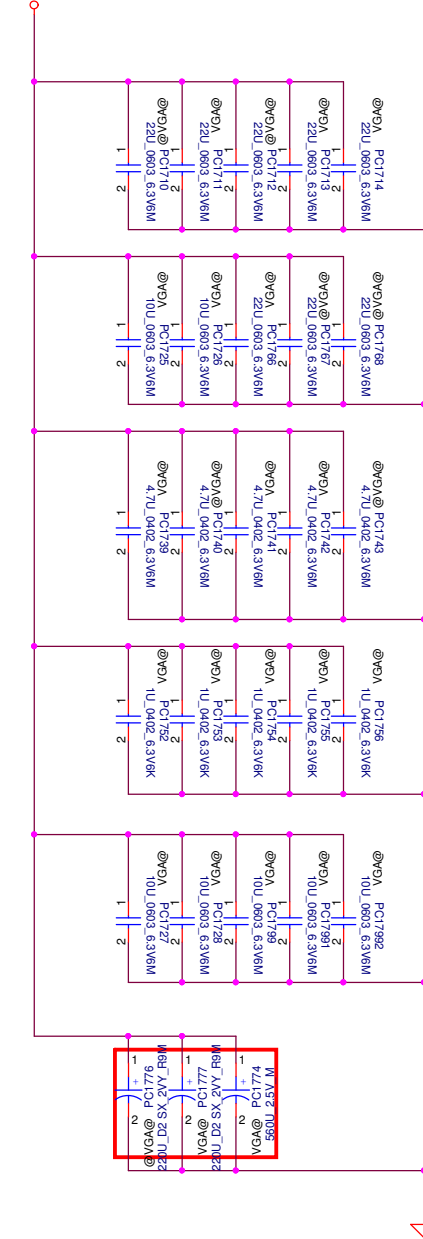
Compal Electronics, Inc.			
Title PWR VGA UP9511P			
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+VGA_CORE



+VGA_CORE			
560uF_OS	X	2	
220uF_D2	X	3(+1@)	
22uF_0805	X	0(+3@)	
22uF_0603	X	27(+8@)	
10uF_0603X		16	
4.7uF_0402	X	20(+7@)	
1uF_0402	X	14	

+VGA_CORE



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		Size		Document Number		C5MMH M/B LAE911P				Rev 0.1
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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Update	Solution Change	0.2	50	Change the PQ310 from AON6366E (SB00001D800) to EMB04N03H (SB00001C500). Change the PQ311 P Q812 from AON6366E (SB00001 b800) to AON7380 (SB00001 G M00). Change the PC302 PC303 PC304 PC311 PC312 from 10U_0603_25V (SE00000X200) to 10U_0805_25V (SE00 0000000). Delete the PC323 10U_0603_25V (SE00000X200).	10/13	A2
02	Design Update	Solution Change	0.2	53	Change the PR603 (10K_0402_1%, SD034100280) from pop to un-pop.	10/13	A2
03	Design Update	Solution Change	0.2	54	Change the PR7126 (100K_0402_5%, SD028100380) from un-pop to pop. Change the PR7126.2 net from +3VS to +3VALW.	10/13	A2
04	Design Update	Solution Change	0.2	63	Change the PC1748 PC1761 PC1770 PC1772 PC1767 PC1768 (22U_0603_6.3V, SE0 0000M000) from pop to un-pop.	10/13	A2
05	Design Update	Down size for SNB MLCC	0.2	50、59、62	Change the PC315 PC1308 PC152 PC152 PC152 from 680P_50V_K_X7R_0603 (SE025681K80) to 680P_50V_K_X7R_0402 (SE074681K80).	10/13	A2
06	Design Update	Solution Change	0.2	59	Change the PQ1302 from 2N7002KW (SB000009Q80) to L2N7002WT1G (SB000005T00).	10/13	A2
07	Design Update	Down size for MLCC	0.2	59	Change the PC1307 from 1U_6.3V_M_X5R_0603 (SE107105M80) to 1U_6.3V_K_X5R_0402 (SE000000K80).	10/13	A2
08	Design Update	Down size for EMI MLCC	0.2	48	Change the PC102 from 100P_50V_J_NPO_0603 (SE024101J80) to 100P_50V_J_NPO_0402 (SE071101J80). Change the PC104 from 1000P_50V_K_X7R_0603 (SE025102K80) to 1000P_50V_K_X7R_0402 (SE074102K80).	10/13	A2
09	Design Update	Down size for MLCC	0.2	63	Change the PC1747 PC1759 PC1779 PC1788 PC1764 PC1766 P from 22U_6.3V_M_X5R_0805 (SE000000I10) to 22U_6.3V_M_X5R_0603 (SE000000M00).	10/13	A2
10	Design Update	Solution Change	0.2	56	Change the PH8103 PH8104 from 150K_5%_0402_B25/50_4500K (SL200002K00) to 220K_5%_0402_B25/50_4700K (SL200002I00). Change the PR8109 PR8110 from 8.87K_0402_1% (SD034887180) to 8.66K_0402_1% (SD034866180). Change the PR8118 PR8119 from 931K_0402_1% (SD034931280) to 57.6K_0402_1% (SD034576280).	10/23	A2
11	雷雕區	Down size for Jump	0.2	53	Change the PJ602 from 43X79 to 43X39.	10/23	A2
12	Design Update	Solution Change	0.2	56、57	Change the PC8113 PC8124 PC8130 PC8159 PC818 from 0.47U_16V_Z_Y5V_0402 (SE000002F80) to 0.47U_6.3V_K_X5R_0402 (SE124474K80). Change the PC8310 from 0.47U_25V_K_X5R_0402 (SE00000WA00) to 0.47U_6.3V_K_X5R_0402 (SE124474K80).	10/25	A2
13	Design Update	Solution Change	0.2	58	Add the location PC9164 PC9165 PC9166 and pop. 22U_6.3V_M_X5R_0603 (SE0000 0M00)	10/26	A2
14	Design Update	CPU transient test result	0.2	56、57、58	Change the PR8114 from 6.81K_0402_1% (SD034681180) to 5.76K_0402_1% (SD034576180). Change the PR8113 from 2.49K_0402_1% (SD034249180) to 1.8K_0402_1% (SD00000R580). Change the PR8117 from 560K_0402_1% (SD034560380) to 442K_0402_1% (SD034442300). Change the PR8116 from 510K_0402_1% (SD00000RK80) to 402K_0402_1% (SD034402380). Change the PR8141 from 100_0402_1% (SD034100080) to 8.2K_0402_1% (SD000004100). Change the PR8149 from 1.05K_0402_1% (SD00000J480) to 3.16K_0402_1% (SD000006580). Change the PR8176 from 20K_0402_1% (SD034200280) to 16.9K_0402_1% (SD034169280). Change the PR8310 from 63.4K_0402_1% (SD03463K280) to 59K_0402_1% (SD034590280). Change the PR8319 from 24.9K_0402_1% (SD034249280) to 22K_0402_1% (SD034220280). Change the PR8325 from 0_0402_5% (SD028000080) to 300_0402_1% (SD034300080). Change the PR8328 from 22K_0402_1% (SD034220280) to 20K_0402_1% (SD034200280). Change the PR8333 from 680_0402_1% (SD034680080) to 300_0402_1% (SD034300080). Change the PC8312 from 270P_0402_50V7K (SE074271K80) to 330P_0402_50V8J (SE000006I80). Change the PR8331 from 470_0603_1% (SD014470080) to 576_0603_1% (SD014576080). Change the PR8336 from 42.2_0402_1% (SD00000ZNO0) to 255_0402_1% (SD034255080). Change the PR8134 from 121K_0402_1% (SD034121380) to 13.3K_0402_1% (SD034133280). Change the PR8138 from 49.9K_0402_1% (SD034499280) to 26.7K_0402_1% (SD034267280). Change the PR8147 from 3.32K_0402_1% (SD034332180) to 768_0402_1% (SD00000TT80). Change the PC9110 PC9108 from 22U_0603_6.3V6 M (SE00000 M000) to un-pop Change the PC9112 PC9113 from un-pop to 22U_0603_6.3V6 M (SE00000 M000) Change the PC8126 from 330P_0402_25V8J (SE00000FD80) to 330P_0402_50V8J (SE000006I80). Change the PR8173 from 0_0603_5% (SD013000080) to 10_0603_1% (SD014100A80). Change the PC8137 from 330P_0402_25V8J (SE00000FD80) to 270P_0402_50V7K (SE074271K80). Change the PC9159 PC9160 from 22U_0603_6.3V6 M (SE00000 M000) to un-pop Change the PC9057 PC9058 from un-pop to 22U_0603_6.3V6 M (SE00000 M000)	10/27	A2
15	Design Update	Power sequence	0.2	59、60	Change the PR1303 from 10K_0402_1% (SD034100280) to 1K_0402_1% (SD034100180). Change the PR1401 from 10K_0402_5% (SD028100280) to 4.7K_0402_5% (SD028470180).	11/02	A2
16	Design Update	Solution Change	0.2	61	Change the PU1201 from UP9511P (SA00009SW00) to UP9511Q (SA00000BK300). Change the PR1243 PR1247 from 10K_0402_5% (SD028100280) to 100K_0402_5% (SD028100380).	11/08	A2
17	Design Update	Solution Change	0.2	52、56、57	Change the PC8317 PC509 PC517 from 1U_0402_10VK (SE0000 0Q10) to 1U_0201_6.3V6K (SE00000YB00). Change the PC8112 PC8115 PC818 PC819 PC857 PC8161 from 1U_0402_25V6K (SE000010V00) to 1U_0201_6.3V6K (SE00000800).	11/08	A2
18	Design Update	Solution Change	0.2	50、56	Change the PR340 P Q814 P Q81A PC83B PC827 PC807 PC808 from pop to un-pop Change the PR326 from un-pop to 0_0603_5% (SD013000080) Change the PR310 from 51.1K_0402_1% (SD034511280) to 52.3K_0402_1% (SD034523280) Change the PC8147 from 10U_0805_25V_X5R (SE00000GK00) to un-pop	11/14	A2

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
19	Design Update	Solution Change	1.0	50	Change the PC313 PC314 from 1 U_16V_X5R_0402 SE000000U000 to 1 U_6 3V_X5R_0201 (SE00000YB00).	12/15	C
20	Design Update	Solution Change	1.0	50、55 56、57	Change the PR304 PR314 PR316、PR22、PR34、PR111、R8120、PR8128、PR8139、PR812、PR813、PR853、PR8154、PR8155、PR8165、PR8170、PR8175、PR890、PR8129、R8163、PR8184、PR8198、PR820、PR808、PR826、PR839、PR8341、PR8342、PR836、PR87、PR333 from 0_0402_5%(SD028000080) to R-short	12/15	C
21	Design Update	Solution Change	1.0	50	Change the PC305 PC324 from 01 U_0402_25V7K(SE00000 W210) to 01 U_0402_25V6(SE00000G880).	12/18	C
22	Design Update	Solution Change	1.0	56	Change the PC8101 PC8122 PC815、PC850、PC8158 from 0.1U_0603_50V7K(SE025104K80) to 0.1U 25V K X7R 0603 (SE042104K80).	12/18	C
23	Design Update	SW2 un-pop	1.0	49	Change the PR217 from un-pop to 0_0402_5%(SD028000080).	12/18	C
24	Design Update	Solution Change	1.0	50	Change the PR326 PR7202 from 0_0603_5% SD013000080) to R-short	12/18	C
25	Design Update	Solution Change	1.0	56	Add PC8116 PC8118 33U_01_25V M_R6 M(SG A0000 A400), and un-pop	12/19	C
26	Design Update	4S_BATT	1.0	50	Delete location PR326 PR327 PC307、PC8 Add location PR338->2M_0402_1%(SD034200480) PR339->100K_0402_1%(SD034100380) Add location PQ315->LTC015EUBFS8TL(SB000011K00) P Q816->2N7002K W1 N SOT323-3 (SB00000ST00)	12/20	C
27	Design Update	Solution Change	1.0	50	Change the PC309 from 0.22U_0603_25V(SE0000005Z80) to 0.47U_0402_16V(SE0000002F80).	12/21	C
28	Design Update	ACIN_CHG	1.0	50	Change the PR306 from 392K_0402_1%(SD034392380) to 499K_0402_1%(SD034499380). Change the PR310 from 52.3K_0402_1%(SD034523280) to 66.5K_0402_1%(SD034665280).	12/25	C
29	Design Update	Power sequence	1.0	60	Change the PR1406 from 10K_0402_1%(SD034100280) to 0_0402_5%(SD028000080).	12/27	C
30	Design Update	3valw interfere	1.0	55、59	Change the Jump PJ7202 PJ1301 from mshort to open Change the bead PL7201 PL1301 from un-pop to pop 0805_5A(S M01000U600). Change the PR7203 from un-pop to pop 4.7_1206_5%(SD001470B80) Change the PC7203 from un-pop to pop 680pF_0402_50V (SE074681K80)	01/10	C
31	Design Update	Solution Change	1.A	55	Change the PR7202 from R-short to 0_0603_5%(SD013000080).	01/12	C

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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	29	Design Update	9/27	power source optimization	DGPU1.8V power source change to 1.8VALW	A2	0.2
2	39	Design Update	9/27	version upgrade	Change board ID to DVT (V15_ID1/VX15_ID11)	A2	0.2
3	37	Design Update	10/17	CNVI power request	Add RM44 for +3VALW to +3VS_WLAN	A2	0.2
4		Design Update	10/19	0 ohm part count reduce	RH186/RH47/RH103/RH105/RH97/RH98/RH99/RH100/ RD3/RD6/RD2/RD15/RD13/RD17/RM22/RM23/RM24/ RM25/RM26/RM27/RM28/RM29/RM30/RM31/RM32/ RM33/RM34/RM35/RM38/RM39/RM40/RS1/RS8/RS16/ R19/R20/RQ5/RQ9/RQ6	A2	0.2
5	41,42	Design Update	10/19	USB common voltage footprint update	LS1/LS10 change footprint to "MURAT_DLM0NSN900HY2D_4P"	A2	0.2
6		Design Update	10/24	for cost, change 10uF_0402 to 0603	CV75, Cv83, CV86, Cc88, CV87, Cv83, Cv73, Cv82,Cv108, Cv119, Cv118, Cv110, Cv120, Cv121, Cv114, Cv115, , CC75, Cc73, Cc80, CC74,CC76, CC78, CC79, CX1 CX3, CA6, CA8, CA9, CA16, CA17, CC71, CC72, CC81, CC89, CC90,	A2	0.2
7	44	Design Update	10/25	USB CMC move to M/B	add L11/ L12 for USB2.0 CMC	A2	0.2
8	39	Design Update	10/26	CNVI device detect issue	add PU 100K RB78 for CNVI card detect reserved RB79 PD 0ohm for CNVI card detect EC add PIN89 GPIO50 as CNVI_DET# add PIN 19 CNVI_DET#	A2	0.2
9	38	Design Update	10/26	for reserve 4 dmic	Change JDMIC1 to 4pin : SP02000TI00	A2	0.2
10	43	Design Update	11/02	SATA HDD redriver EQ tuning	UNPOP RO17 for redriver EQ	A2	0.2
11	25	Design Update	11/02	NV vga sequence tuning	change RV105 to 8.2K (vga_core_en) RV12 change to 100k_1% (1.35VSDGPU_PWR_EN) RV113 change to 4.7k_5% PR1303 change to 1k PR1401 change to 4.7k	A2	0.2
12	43	Design Update	11/06	co-lay no HDD re-driver circuit	add CO14/CO16~18/RO21~24 for no re-driver.	A2	0.2
13	45	Design Update	11/13	for factory request, don't include SW1 in bom	unpop SW1 and control by SMT memo	A2	0.2
14	40	Design Update	11/13	replace level shift by 0 ohm on Type-C circuit	unpop QS1/RS107/RS108 POP RS114/RS115	A2	0.2
15		Design Update	11/13	fine tune crystal frequency	24Mhz Keep 33 18 /1M 25Mhz Keep 10 18 /330 27Mhz CV1 change to 15PF (15 12 /0) 32.768Khz change CH7/CH8 to 10PF (10 10 /10M)	A2	0.2
16		Design Update	12/14	0 OHM change to R-short	change RC17/RH5/RH6/RH94/RH96/RV125/RM2/RB19/RB76/RO4 /RS114/RS115 to R-short	PVT	1.0
17	18	Design Update	12/14	peci issue, can't get system temperature	UNPOP RH41	PVT	1.0
18	46	Design Update	12/14		unpop SW2(BI SW)	PVT	1.0
19	39	Design Update	12/16		change board ID to ver1.0 (V series 15k/ vx series 200k)	PVT	1.0
20	40	Design Update	12/18	change typeC VCONN sol to G527	add RS116 on VBUS_EN_179 change US2 to SA00006Y700, add RS156/RS155/CS101/CS124	PVT	1.0

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